

UNIVERSAL ASSEMBLER VERSION 2.2.B JULY 29, 1979 (IN-HOUSE)

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17 attaches

143 r/s'd

3802

code

script

BLKIN⁰⁹⁷⁷ @ 177

Trim!

not 171 where should be.

- 1. . 2.14.G HJS 79 NOV 27 INSERT TIMING & DMP I/O INTERFACE
- 2. . 2.14.F HJS 79 OCT 10 CHANGE TO HONEYWELL NOISEMAKER (SOUNDS BETTER)
- 3. . 2.14.E HJS 79 AUG 13 FINAL CLEANUP (& BUG FIX) BEFORE RELEASE
- 4. . 2.14.D HJS 79 AUG 10 FOUND BUGS AND FIXED THEM
- 5. . 2.14.C HJS 79 AUG 6 FINAL CLEANUP BEFORE TRY THIS VERSION
- 6. . 2.14.B HJS 79 APR 17 RE-ORGANIZE ROUTINES TO MAKE IT FIT
- 7. . 2.14.A HJS 79 APR 4 START MODIFICATIONS FOR INTERNAL RIM 3800
- 8. *
- 9. . 2.13.A HJS 79 JAN 22 FIX REGS TO WORK WITH ACCESS PROTECTED STACK
- 10. *
- 11. . 2.12 HJS 78 OCT 16 FINAL RELEASE
- 12. . 2.12.D HJS 78 OCT 15 CHANGE SYSTAT SO CAN TELL THE PRE-RELEASE LEVEL
- 13. . 2.12.C HJS 78 OCT 12 CORRECT THE PC FOR MEMORY FAULTS TO MATCH 6600 PC
- 14. . 2.12.A HJS 78 SEP 05 REFORMAT, RECOMMENT & FIX STACK FOR ACCESS ENABLE
- 15. . 12 THE NUMBER IS OCTAL!! TO MATCH DEBGU ? DISPLAY
- 16. *
- 17. . 2.9 HJS 78 JUL 20 FINAL RELEASE OF VERSION 9
- 18. . 2.9.K HJS 78 APR 23 SPLIT PROC, MAKE RELOCATABLE, CHANGE APF, ADD AML
- 19. . 2.9.J HJS 78 MAR 20 RESTRUCTURE INTERRUPT SEQUENCE & MINOR MODS
- 20. . 2.9.I HJS 78 FEB 27 CORRECT 9.H FOR FAULT CLEANUP
- 21. . 2.9.H HJS 78 FEB 16 EVERYBODY MEMPF'S, KEYBOARD SCAN, & SIR CHANGE
- 22. . 2.9.G HJS 78 FEB 3 CORRECT TIMING, COMMENTS, & ADD POR TIMEOUT
- 23. . 2.9.F HJS 78 JAN 11 FIXING MIN/MOUT TIMINGS
- 24. . 2.9.E HJS 78 JAN 4 TESTING REPEATED KEYIN CONTROLS
- 25. . 2.9.D HJS 77 DEC 21 CORRECT STL INSTRUCTION
- 26. . 2.9.C HJS 77 DEC 13 BACK OFF FROM KBD RPT & RE-DO STL FOR TIMING
- 27. . 2.9.B HJS 77 NOV 20 INCLUDE TIMINGS AS CALCULATED & FIX MINOR BUGS
- 28. . 2.9.A HJS 77 NOV 14 CHANGE KEYBOARD CODE TO AID REPEATED KEY CONTROL
- 29. *
- 30. . 2.8.B HJS 77 SEP 22 MTI CHANGE SO LENGTH IS 2 BYTE NUMBER
- 31. . 2.8.A HJS 77 SEP 19 MTI CHANGE TO ALLOW MFRPT ON ANY INTERRUPT
- 32. *
- 33. . 2.7. HJS 77 SEP 7 MINOR BUG-FIX AND OPTIMIZATION FOR RELEASE
- 34. *
- 35. . 2.H.B HJS 77 AUG 31 MTI SPECIAL VERSION
- 36. *
- 37. . 2.5.C HJS 77 AUG 16 UPDATE COMMENTS ON THE CODE
- 38. . 2.5.B HJS 77 JULY 13 CORRECTED NAMES FOR COM REGISTERS
- 39. . 2.5.A HJS 77 JULY 12 UP TO NEXT NEW VERSION NUMBER
- 40. *
- 41. . 2.4.B HJS 77 JULY 12 FIXED ILLEGAL MAR CHANGE IN REGL RETURN TO FETCH
- 42. . FIXED FILE TO CONFORM TO VRP FORMAT (A LITTLE)
- 43. . 2.4.A HJS 77 JULY 7 INITIAL PRE-RELEASE OF THE MICRO-CODE

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83.
1.A
10.A
11.A

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. USEFUL INFORMATION TO BE PASSED ON:
*
. *****
. IF SECTOR CONTAINING SEKBS1 IS WRITE PROTECTED THEN CAN NOT DO A RESTART!!!!
. *****
. THE FOLLOWING TIMING RESTRICTIONS APPLY TO MEMORY OPERATIONS:
. SMR & MDW TO MWAIT : 100 NS MINIMUM BEFORE THE MWAIT TEST PERFORMED
. SMR & MDW -> MWAIT : 450 NS WITH NO INTERVENING IMAR, DMAR, OR XX2MR
. IMAR & DMAR -> SMR & MDW : 200 NS
. MAROH -> SMR & MDW : 100 NS
. MAROL -> SMR & MDW : 000 NS
. MWAIT -> MDR : 100 NS (THIS DONE BY MEMPF CHECK!)
. *****
. ALL SMR'S AND MDW'S MUST HAVE FOLLOWING MWAIT ,MEMPFX EVERYWHERE
. IN THE CODE EVEN IF MWAIT ,s+1 IS USED (IGNORING MEMORY FAULT)
. *****
. FOR TESTING MEMPF, CHANGE MWAIT MACRO TO BE JT,MP s+1 <<<
. CODE THERE, TESTABLE AS USED BUT NO EFFECT!!
. *****
. EACH SERVICE ROUTINE THAT USES THE MAR MUST HAVE A MWAIT ,s+1 BEFORE THE
. MAR CHANGED, AND MUST CLEAR (TEMPORARILY) SWUSER IF USED.
. RETURN THROUGH SRVNXT.
. *****
. ALL INPUTS FROM A PORT INSTRUCTION SHOULD BE LOGICAL (OUTPUT CAN ONLY BE
. LOGICAL OR 'IT').
. ARITHMETICS MAY BE DONE ON INPUTS WITH CAUTION. ONLY IF THE DATA HAS NO SETUP
. TIME, i.e. MDR IS OK, BUT IMPI OR URI ARE NO-NO'S.
. *****
. DELAY AROUND SECTOR TABLE WRITES IS NOT NECESSARY.
. *****
. FOR A FONT LOAD MUST DO: 1) SDLM, 2) SKCH'S AS NEEDED, 3) THREE WAISTED
. SLDCH - RLDCH PAIRS TO SET UP COUNTER CORRECTLY, 4) SEVEN SETS OF SLDCH -
. RLDCH WITH THE DATA IN MAROL, 5) FINALLY RLDM AT THE END
. NOTE: THE DELAY FROM SLDCH TO RLDCH MUST BE AT LEAST 200 NSEC. IN ALL CASES
. AND MAROL MUST NOT CHANGE DURING THIS TIME. EXTRA RLDCH'S DO NOT HURT.
. *****

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INC PROCINC
SNAPOPT -X
SNAPOPT X
INC PROC14G3.PORTASGN PORT ASSIGNMENT DISPLAY

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MICRO-PROCESSOR EMULATION SUPPORT CODE - HJS - 79DEC12 16:20
 . THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS

3.H
 4.H
 5.H
 6.H
 7.H
 8.H
 9.H
 10.H
 11.H
 12.H
 13.H
 14.H
 15.H
 16.H
 17.H
 18.H
 19.H
 20.H
 21.H
 22.H
 23.H
 24.H
 25.H
 26.H
 27.H
 28.H
 29.H
 30.H
 31.H
 32.H
 33.H
 34.H
 35.H
 36.H
 37.H
 38.H
 39.H
 40.H
 41.H
 42.H
 43.H

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*
. PORT
. SUB 0 1 2 3 4 5 6 7
. 0 0 LIREG LIMP BASW MODW STW LUF LUCF
. 0 I
. 0 0 IIMP DIMP COMF CHUF IMAR DMAR
. 10 I
. 1 0
. 0 I SRVREQ STATUS IDCODL IDCODH UCFLG MDR STEK
. 1 0 RIMDATO MDW LSPKR RIMADRO LDRIMBP SLDCH RLDCH
. 10 I
. 2 0 LDMAP SKCH SDLM KBSC RDLM CMPF SMR
. 0 I KBDD EXCOM17 RIMDATI RIMSTAI EXCOM11 EXCOM12 EXCOM14 EXCOM15
. 2 0 DMPADH DMPADL DMPDIO
. 10 I DMPRDS DMPDTI ???STS??
. 3 0 URFO
. I
. 4 0 URO (MR2XXL)
. I MARIL
. 5 0 URO (MR2XXH)
. I MARIH
. 6 0 MAROL (XX2MRL)
. I URI
. 7 0 MAROH (XX2MRH)
. I URI
.
. USER IO PORTS 4-7
. REGS 0 URA URB URC URD URE URH URL URX
. 10 PCH PCL SPH SPL PSW I35 I02 IMP
    
```


12.I
 13.I
 14.I
 15.I 020002
 16.I 020003
 17.I 020004
 18.I 020005
 19.I 020006
 20.I
 21.I
 22.I
 23.I 010002
 24.I
 25.I 010000
 26.I 010001
 27.I 010002
 28.I
 29.I
 30.I
 31.I
 32.I
 33.I
 34.I
 35.I 010015
 36.I
 37.I
 38.I
 39.I
 40.I
 41.I 030000
 42.I 030001
 43.I 030002
 44.I 030001
 45.I 030002
 46.I
 47.I
 48.I
 49.I
 50.I
 51.I
 52.I
 53.I
 54.I
 55.I
 56.I
 57.I
 58.I
 59.I
 60.I
 61.I
 62.I
 63.I

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*
. CONDITION CODES
.
MO      EQU      F6+2      MEMORY READY
MP      EQU      F6+3      MEMORY FAILURE (OF ANY SORT!)
IZ      EQU      F6+4      IMPLICIT REGISTER ZERO
IO      EQU      F6+5      IMPLICIT REGISTER ODD
BR      EQU      F6+6      BUS READY (MICRO-BUS ONLY)
*
. REGISTER ALLOCATION
.
Q        EQU      F5+02      NOBODY SHOULD DO WRITE'S TO Q
.
PDLNP   EQU      F5+0        DISPLAY LINE POINTER
KBSCNT  EQU      F5+01      KEYBOARD SCAN COUNTER
SCANSV  EQU      F5+02      KEYBOARD SAVED SCAN NUMBER, REPEATED AI
*
. DISKETTE INTERFACE
.
.          F5+03 .. F5+013
.          F5+014 (FREE)
*
. AUDIO CHANNEL CONTROL REGISTER
.
ACD      EQU      F5+015     AUDIO CHANNEL ATTEN/VALUE
.ACPL    EQU      F5+016
.ACPH    EQU      F5+017     AUDIO CHANNEL CONTROL & MSB POINTER
*
. TEMPORARIES - AVAILABLE IN ANY ROUTINE, LOST BETWEEN ROUTINES
.
LINK     EQU      F5+F6+00   SUBROUTINE CALL AND RETURN LINKAGE REGS
TEMP1    EQU      F5+F6+01   PROCESSOR EMULATION TEMPORARIES
TEMP2    EQU      F5+F6+02
TEMPH    EQU      TEMP1      H & L ONLY FOR DOUBLE H/L MACROS
TEMPL    EQU      TEMP2
*
. COMMUNICATION PORT REGISTER ALLOCATIONS
.
.          F5+F6+03 .. 017
*
. CAPABILITY BITS:
. THESE BITS DEFINE THE VERSION OF THE 1800/3800 PROCESSOR THAT THIS IS FOR
.
.   XX XXX XXX
.       0 --- MICRO I/O BUS AVAILABLE
.       1 ---- COMMUNICATIONS INTERFACE (MULTIPOINT) ASYNC.
.       2 ----- 1800 SINGLE/DOUBLE DISKETTE DRIVE AVAILABLE
.       3 ----- APF SPECIAL MICRO-BUS INTERFACE AVAILABLE
.       4 ----- DMP I/O INTERFACE INSTRUCTIONS AVAILABLE
.       5 ----- INBOARD RIM AVAILABLE
.       6 ----- 5500 I/O BUS AVAILABLE
.       7 ----- COMMUNICATIONS INTERFACE AVAILABLE (ASYNC, BISYNC, & SDLC)
    
```


. EXTENDED CONDITIONS, AND SYSTEM REGISTER DEFINITIONS

64.I	000000	CAPMICR	EQU	B0-B0	NOT AVAILABLE
65.I	000000	CAPIMA	EQU	B1-B1	IMA BIT HERE !!
66.I	000000	CAPBLUE	EQU	B2-B2	NOT AVAILABLE
67.I	000000	CAPAPF	EQU	B3-B3	NOT AVAILABLE
68.I	000020	CAPDMP10	EQU	B4	SPECIAL CODE FOR DMP BUS INCLUDED
69.I	000040	CAPRIM	EQU	B5	ONLY INBOARD RIM AVAILABLE
70.I	000000	CAP5510	EQU	B6-B6	NOT AVAILABLE (EXCEPT INBOARD RIM)
71.I	000000	CAPCOM	EQU	B7-B7	NOT AVAILABLE
72.I		.			
73.I	000060	CAPABILI	EQU	CAPCOM+CAP5510+CAPRIM+CAPDMP10+CAPAPF+CAPBLUE+CAPIMA+CAPMICR	
74.I		*			
75.I		.			
76.I		.			
77.I	000000	PROC	EQU	00<9	EMULATION SUPPORT CODE IN ROMS 0 & 1
78.I	002000	PROD	EQU	02<9	EMULATION SUPPORT CODE IN ROMS 2 & 3
79.I	004000	FLEX	EQU	04<9	MICRO-BUS CODE IN ROMS 4 & 5
80.I	006000	CDOX	EQU	06<9	COMM TRANSMIT CODE IN ROM 6
81.I	007000	CDOR	EQU	07<9	COMM RECEIVE CODE IN ROM 7
82.I		.			
84.			IFNE	TYPE,3	
86.			XIF		
87.		.			
88.	000000	PROCL	ORG	PROC	LOGICAL SPACE IN ROM'S
89.	000000	PROCP	ORG	0	PHYSICAL SPACE DONE AT LINK TIME
90.	000000	PROCL	USE	PROCL	ENABLE BOTH ADDRESS SPACES
91.	000000		USE	PROCP	BUILD CODE IN PHYSICAL SPACE
92.	000000L	PROCP	LOC	PROCL,2	LOC'ING TO LOGICAL ADDRESSES

```

95.
96. 000000L
97.
98.
99.
100. 000000L 01011001 11111111
101.
102. 000001L 11000100 11111110
103. 000002L 00110111 01000110
104.
105. 000003L 01010001 00000000
    000004L 00110111 10001100
106. 000005L 00110111 00000100
107. 000006L 00110111 00000011
108. 000007L 00000111 11111101
109. 000010L 00000111 11110001
110. 000011L 00110111 01000100
111.
112. 000012L 01010001 10011100
    000013L 00000111 10110000
113. 000014L 01010001 00100100
    000015L 00110111 10001001
114. 000016L 00110001 00110111
    000017L 01000101 00000010
115. 000020L 11000010 11011010
116.
117.
118.
119. 000021L 01010001 00001100
120. 000022L 00110111 11100000
    000023L 00110111 00000101
121. 000024L 01010010 00010000
122. 000025L 11000000 11101101
123.
124. 000026L 01010001 11110000
    000027L 00110111 00000101
125. 000030L 01010001 11101111
    000031L 00110111 11100000
126. 000032L 01010001 00000000
    000033L 00110111 11000000
127. 000034L 01101111 11110010
128.
129. 000035L 00110111 00101001
130. 000036L 01110001 11110010
    000037L 01101110 01110010
131. 000040L 01010001 00000000
132. 000041L 11000100 11011110
133. 000042L 00110111 00001100
134. 000043L 11000000 11100010
    
```

*
 POR:

. INITIALIZE ALL CONTROL TABLES THAT CAN NOT BE INIT'D BY POR MACRO CODE

```

    BPGX      $
    STB       RDLM          DO NOT CLEAR UP THE DISPLAY
    MWAIT     ,IGNORE      TIMEOUT SAFETY (IGNORE MEMORY FAULT)
    STB       CMPF         (INSTEAD OF FAULT JUMP)
    LDPI      PSWO,0       T-REG IS ZERO FOR THE FOLLOWING
                                SET EMULATION PSW
    LDPT      MODW         PORT CONTROLS APPROPRIATLY
    LDPT      BASW         BASE REGISTER IS INITIALLY ZERO
    LDRT      ACD          NO AUDIO CHANNEL INITIALLY
    LDRT      KBSCNT       SAVE THE SCAN NUMBER AND
    LDPT      KBSC         START THE FIRST KEY SCAN
    LDRT      STMOD475
    LDRI      PDLNP,SEDLBOT,CC POINT TO THE BOTTOM LINE
    LDPI      PCOL,SRTMOUT ASSUME THAT A TIMEOUT WILL HAPPEN
    TSTIP     ,STLIMOUT,STEK CHECK IF IT DID
    BRA       POROUT,FZ    YES, DON'T INIT STL OR MEMORY
. MUST INIT SECTOR TABLE & ZERO SYSESR OR IMMEDIATE RESTART OR MEMPF
    LDRT      STAE+STWE    INIT WHOLE SECTOR TABLE
    PORLST    LDPT        MAROH,STW
    DOTI     ,AC,16       LOOP TILL ALL ARE ACCESS & WRITE ENABLE
    BRA      PORLST,FC
    LDPI     STW,SYSPROM>8.AND.0360 SECTOR 017 IS SYSTEM ROM, PROTECT IT
    LDPI     MAROH,SYSESR>8 POINT TO THE EMULATION SUPPORT PAGE
    LDPI     MAROL,SYSESR  START OF IT (T-REG IS ZERO)
LDRT     TEMPL         INITIALIZE THE COUNTER
    PORZRO   LDPI MDW, φ ZERO THE NEXT BYTE (T-REG IS ZERO)
STB      INCR TEMPL,TEMPL COUNT ALL OF THE BYTES IN THE PAGE
    LDRT     0           DATA TO BE WRITTEN IS ZERO
    MWAIT    ,IGNORE    !! IGNORE ANY AND ALL FAULTS !!
    STB     IMAR, LDTP MARIL
    BRA     PORZRO, FC CONTINUE TILL ALL PAGE DONE
    FZ
    
```

. POWER ON RESTART, INITIALIZE THE WORLD

135.
 136. 000044L 00110111 10001001
 137.
 138. 000045L 01010001 11110000
 000046L 00110111 10001000
 139.
 140.
 141.
 142.
 143. >000047L 01011001 11111111
 >000050L 11001111 11111111
 144.

*
 FETPC LDPT PCOL LOAD THE PC LSB ADDRESS

POROUT LDPI PCOH, SYSROM>8

. NOTE: *COPT MAROTH, STW* NORMALLY HERE, PCL IS ZERO AND PCH = SYSROM>8
 . THIS GENERATES A POINTER TO SRPOWER-UP VECTOR ENTRY

BRAX RETS OK, MICRO-POR DONE, DO MACRO POR

(OR TIMEOUT) (OR SC ERROR)

*TSTIT, SW61K
 BRA KBD\$DO, T2
 LOPI MAROH, SYSRAM>8
 LOPR STW, SST16E
 LOPI MAROH, SYSCONA>8
 LOPR STW, SST15E
 BRA KBD\$DO*

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147.
148. 000051L
149.
150. 000051L 01010001 11001110
    000052L 01101111 11110000
151. 000053L 11000100 11010100
    000054L 11000111 00100111
152. 000055L 00110001 11011100
    000056L 01010101 11111011
    000057L 00110111 00000100
153. 000060L 11001111 10100100
154.
155. 000061L 00110001 00110001
    000062L 01000010 10000000
156. 000063L 00010001 11110000
157. 000064L 11000000 10111100
158.
159. 000065L 11000100 11001010
    000066L 11000111 00100111
160. 000067L 01010001 01101011
    000070L 00110111 11000000
    000071L 00110111 01000111
161. 000072L 01010001 00000000
162. 000073L 11000100 11000100
    000074L 11000111 00100111
163. 000075L 00110010 00110110
    000076L 00110111 00101001
164. 000077L 00010001 10111101
165. 000100L 11000011 10111101
166. 000101L 00000110 01111101
167. 000102L
168. 000102L 01010001 10011100
169.
170. 000103L 11000100 10111100
    000104L 11000111 00100111
171. 000105L 00110111 11000000
    000106L 00110111 01000111
172. 000107L 01010100 00000010
173. 000110L 01000100 01101110
174. 000111L 11000000 10110100
175. 000112L 01010001 10011100
176. 000113L 00000111 11110000
177. 000114L 11000100 10110011
    000115L 11000111 00100111
178. 000116L 00110111 00001100
179. 000117L 00110001 00110110
    000120L 01101111 11110001
180. 000121L 00110111 01000111
181. 000122L 01010001 00101101
    000123L 01101111 11110000
182. 000124L 11000100 10101011
    000125L 11000111 00100111
    
```

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*
DL$DO:
. 4.80 + 2.10 ON BOTLINE
    BAL LINK,DLNL SET UP RETURN FROM KEY SERVICE
    MWAIT ,MEMPFDL WAIT ON WAISTED IFETCH
    DOPIP MODW,ND,-1-SWUSER,PSWI DISABLE USER MODE FOR READ/Writes
    BRA KBD$DO GO DO FIRST KEYBOARD SERVICE
DLNL TSTIP AC,STBOTLN,STATUS SET CARRY IF BOTTOM LINE STATUS
    LDTR PDLNP
    BRA DLNXT,FC NOT YET
    MWAIT ,MEMPFDL WAIT ON KBD STATUS BIT WRITE
    LDPI MAROL,SELFREQ,SMR GET FREQ COUNTER, SAME PAGE AS KBD STUF
    TCLR SET T-REG ZERO (NOTE: CARRY IS TRUE!!)
    MWAIT ,MEMPFDL
    DOPP MDW,AC,MDR ADD ONE AND RESTORE IT
    LDTR ACD,CC ** HONEYWELL AUDIO CHANNEL TIMER **
    BRA DLACNINC,TZ DO NOT INCREMENT OF CHANNEL OFF
    INCR ACD
DLACNINC LDTI SEDLBOT POINT TO THE BOTTOM LINE ON THE SCREEN
DLNXT MWAIT ,MEMPFDL
    LDPT MAROL,SMR SET LSB OF ADDRESS AND READ ADDRESS LSB
    DOTI ,SB,2 SUBTRACT 2 FROM LIST POINTER
    TSTIT SB,SEDLN01 HAVE WE GONE OVER THE TOP?
    BRA DLINEOK,FC IF SO, GO BACK TO THE BOTTOM (SAFETY!)
DLINEOK LDTI SEDLBOT
    LDRT PDLNP
    MWAIT ,MEMPFDL
    STB IMAR
    LDRP TEMP1,MDR GET LSB OF DATA POINTER
    STB SMR GET MSB ALSO
    BAL LINK,DLNLR SET UP RETURN ADDRESS (VERY EARLY!)
    MWAIT ,MEMPFDL
    
```

183. 000126L 00110001 00110110
000127L 00110111 11100000
184. 000130L 01110001 11110001
000131L 00110111 11000000
000132L 00110111 01000001

LDPP MAROH,MDR GET MSB POINTER

LDPR MAROL,TEMP1,LDMAP AND LSB, AND STROBE TO LOAD THE DMA PNT

185. • BRA KBD\$DO GO DO THE SECOND KEYBOARD SCAN

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186.
187. 000133L
188.
189.
190.
191.
192.
193.
194.
195.
196.
197.
198.
199.
200.
201.
202.
203.
204.
205.
206.
207.
208.
209.
210.
211. 000133L 01010001 01101001
      000134L 00110111 11000000
      000135L 01010001 11101111
      000136L 00110111 11100000
212. 000137L 00110001 00110001
      000140L 01000101 01000000
213. 000141L 11000011 10100000
214.
215. 000142L 00010001 10110001
      000143L 01000100 00010000
216. 000144L 11000000 01111000
217.
218. 000145L 00010010 00110001
219. 000146L 01010010 01111000
      000147L 01101111 11110001
220. 000150L 11101111 00000001
221.
222.
223. 000151L 01010001 00000010
224. 000152L 11001111 01101101
225. 000153L 01010001 00000001
226. 000154L 11001111 01101101
227. 000155L 01010001 00000010
228. 000156L 11001111 01101110
229. 000157L 01010001 00001000
230. 000160L 11001111 01101110
231. 000161L 01010001 10000000
    
```

+
 KBD\$DO
 . * * * 4.75 * * * NEW KEY JUST WENT DOWN
 . 2.95 THE KEY IS UP AND WAS NOT LAST TO GO DOWN
 . 4.85 REPEATED KEY UP
 . 4.65 REPEATED KEY DOWN
 . + 0.60 IF <SPACE>, <CANCEL>, <.>, <BACKSPACE>
 . OR + 0.40 IF <ENTER>

 . * * * 4.20 * * * KBKSI STATUS BIT (UP OR DOWN)
 . + 0.15 IF KBKS2
 . + 0.20 IF STATUS BIT DOWN
 . OR 4.35 KBREINT STATUS BIT DOWN
 . OR 5.50 KBREINT STATUS BIT UP
 . OR 5.50 RESTART - IMP ZERO TO SCROM
 . OR 5.85 RESTART - NON-RPT'D INST. TO SCROM
 . OR 6.70 RESTART - RPT'D & IMP NON-ZERO TO SCROM

 . SCAN THE KEYBOARD BY:
 . 1) WAIT FOR THE LAST SCAN TO COMPLETE
 . 2) IF SPECIAL KEY, DO IT'S TYPE OF SERVICE (SET OR CLEAR STATUS BIT)
 . 3) IF NEW CLOSURE GET KEYCODE, SAVE IT, AND SAVE THE SCAN NUMBER
 . 4) IF NOT THE SAME KEY AS SPECIFIED BY LAST SCAN NUMBER THEN DONE
 . 5) IF SAME, AND STILL DOWN, SET STATUS BIT ELSE, CLEAR IT

 DLDPI MARO,SEKBS1 MIDDLE OF 3 BYTES THAT WILL WORK WITH

 KBDWAIT TSTIP ,STKBRDY,STATUS

 BRA KBDWAIT,TZ (LOOPS ONCE ON SECOND SERVICE, MAYBE)
 (NOT READY TILL 5.3 MICRO-S FROM KBSC)
 TSTIR SB,16,KBSCNT,CC IS IT FUNCTION KEY (OR THAT GROUP?)

 BRA KBKEY,FC NO, REGULAR KEY

 DOTR ,AC,KBSCNT,,CO DOUBLE THE NUMBER FOR JUMP TABLE
 DORA TEMP1,AC,KBTBL PUSH A BACKWARDS TABLE OFFSET

 BRR TEMP1 RETURN
 INTO THE TABLE THIS IS TOP OF

 LDTI SEKBDKY 17 KEYBOARD KEY
 BRA KBKS1
 LDTI SEDSPKY 16 DISPLAY KEY
 BRA KBKS1
 LDTI SEFUNC2 15 F2 KEY
 BRA KBKS2
 LDTI SEFUNC4 14 F4 KEY
 BRA KBKS2
 LDTI SEINTKY 13 INTERRUPT KEY

232.	000162L	11001111	01001011	BRA	KBREINT	
233.	000163L	01010001	00010000	LDTI	SEFUNC5	12 F5 KEY
234.	000164L	11001111	01101110	BRA	KBKS2	
235.	000165L	01010001	00000100	LDTI	SEFUNC3	11 F3 KEY
236.	000166L	11001111	01101110	BRA	KBKS2	
237.	000167L	01010001	00000100	LDTI	SEKBRDY	10 . (POINT) KEY
238.	000170L	11001111	01110111	BRA	KBREG	
239.	000171L	01010001	00000100	LDTI	SEKBRDY	7 NO-KEY
240.	000172L	11001111	01110111	BRA	KBREG	
241.	000173L	01010001	00000001	LDTI	SEFUNC1	6 F1 KEY
242.	000174L	11001111	01101110	BRA	KBKS2	
243.	000175L	01010001	01000000	LDTI	SEATTKY	5 ATTENTION KEY
244.	000176L	11001111	01101110	BRA	KBKS2	
245.	000177L	01010001	00100000	LDTI	SERSTKY	4 RESTART KEY
246.	000200L	11001111	01001011	BRA	KBREINT	
247.	000201L	01010001	00000100	LDTI	SEKBRDY	3 SPACE BAR
248.	000202L	11001111	01110111	BRA	KBREG	
249.	000203L	01010001	00000100	LDTI	SEKBRDY	2 BACKSPACE KEY
250.	000204L	11001111	01110111	BRA	KBREG	
251.	000205L	01010001	00000100	LDTI	SEKBRDY	1 CANCEL KEY
252.	000206L	11001111	01110111	BRA	KBREG	
253.	000207L			KBTBL		
254.	000207L	01010001	00000100	KBKEY	LDTI	SEKBRDY
255.				BRA	KBREG	0 ENTER KEY

. DISPLAY - KEYBOARD SERVICE ROUTINES

256.								
257.	000210L	01101111	11110001	+	KBREG	LDRT	TEMP1	
258.	000211L	00110001	00110001			TSTIP	,STKBKC,STATUS	NEW CLOSURE?
	000212L	01000101	00010000					
259.	000213L	11000010	01100001			BRA	KBGET,FZ	YES, DO IT
260.	000214L	00010001	11110001			TSTRR	XR,SCANSV,KBSCNT	SAME AS THE LAST KEY?
	000215L	00010000	11000010					
261.	000216L	11000010	01010001			BRA	KBDON,FZ	NO, FINISHED
262.	000217L	01010001	00001000			LDTI	SEKBDWN	YES, SAME KEY
263.	000220L	11001111	01101101			BRA	KBKSI	CONTINUOUSLY SET THE BIT IF STILL DOWN
264.				.				CLEAR BIT CONTINUOUSLY IF UP
265.				.				IF GOES DOWN AGAIN GET NEW CLOSURE
266.				.				RATHER THAN REPEATED CLOSURE!
267.								
268.				*				
269.	000221L	00110111	00001101		KBKS2	STB	DMAR	POINT TO SEKBKS2
270.								
271.	000222L	01101111	11110001		KBKS1	LDRT	TEMP1	SAVE THE STATUS BITS
272.	000223L	00110001	00110001			LDTP	STATUS	
273.	000224L	00110111	01000111			STB	SMR	GET THE STATUS BYTE
274.	000225L	01000101	00100000			TSTIT	,STKBNS	KEY CLOSED?
275.	000226L	11000010	01010110			BRA	KBCLS,FZ	YES
276.								
277.	000227L	01110001	11110001		KBOPN	DOTIR	,XR,0377,TEMP1	NO, OPEN, TURN THE BIT OFF
	000230L	01010000	11111111					
278.	000231L	11000100	01100110			MWAIT	,MEMPFDL	
	000232L	11000111	00100111					
279.	000233L	00110101	00110110			DOPP	MDW,ND,MDR	BY ANDING IT OUT
	000234L	00110111	00101001					
280.	000235L	11001111	01010001			BRA	KBDON	
281.								
282.	000236L	00110111	00001100		KBGET	STB	IMAR	KEYBOARD CHARACTER SAVE AREA
283.	000237L	11001110	11111111			DELAY	1	
284.	000240L	00110001	01010000			LDPP	MDW,KBDD	OUTPUT THE DATA
	000241L	00110111	00101001					
285.	000242L	00010001	11110001			LDRR	SCANSV,KBSCNT	SAVE THE SCAN NUMBER (FOR REPEATS)
	000243L	00000111	11110010					
286.	000244L	11000100	01011011			MWAIT	,MEMPFDL	** WHAT IF 2ND SCAN SERVICE & LDMAP'D
	000245L	11000111	00100111					
287.				.				ALREADY, IS AN EXTRA ONE OK?
288.	000246L	00110111	00001101			STB	DMAR	POINT BACK TO SEKBS1
289.	000247L	11001111	01010111			DELAY	2	
290.	000250L	00110111	01000111			STB	SMR	
291.	000251L	01110001	11110001		KBCLS	LDTR	TEMP1	GET BIT TO SET
292.	000252L	11000100	01010101			MWAIT	,MEMPFDL	
	000253L	11000111	00100111					
293.	000254L	00110011	00110110			DOPP	MDW,OR,MDR	SET IT
	000255L	00110111	00101001					
294.	000256L	00010001	11110001		KBDON	DOTRR	,IT,Q,KBSCNT,C1	POINT TO THE NEXT SCAN ENTRY (CLEAR)
	000257L	00010110	01110010					
295.	000260L	01010101	00111111			DOPI	KBSC,ND,077	KEEPING THE NUMBER IN RANGE (CARRY ALSO)
	000261L	00110111	01000100					

296. 000262L 00000111 11110001
297. 000263L 11101111 00000000

LDRT KBCNT,CC
BRR LINK

(5.3 MICRO-SEC TIME TILL READY FROM NOW
AND RETURN FROM KEY SERVICE ON ERROR TO

298.					
299.	000264L	00110111	00001101	+	
300.	000265L	01101111	11110001	KBREINT	STB DMAR
301.	000266L	00110001	00110001		LDRT TEMP1 SAVE THE BIT
302.	000267L	00110111	01000111		LDTP STATUS
303.	000270L	01000101	00110000		STB SMR IN SEKBKS2
304.	000271L	11000010	01010110		TSTIT ,STKBKC+STKBNS NEW CLOSURE OR STILL CLOSED?
305.					BRA KBCLS,FZ YES, ITS DOWN, SO SET IT!
306.	000272L	01010001	10100000		LDTI SEINTKY+SERSTKY
307.	000273L	11000100	01000100		MWAIT ,MEMPFDL IT IS UP! SEE IF BOTH KEYS WERE DOWN
	000274L	11000111	00100111		
308.	000275L	00110101	00110110		DOTP ,ND,MDR SELECT RESTART AND INTERRUPT KEYS
309.	000276L	01000000	10100000		TSTIT XR,SEINTKY+SERSTKY WERE BOTH SET?
310.	000277L	11000010	01101000		BRA KBOPN,FZ NO, ONLY ONE
311.	000300L	00110001	00110110		DOPRP MDW,XR,TEMP1,MDR YES, TURN THE BIT OFF & DO A RESTART
	000301L	01110000	11110001		
	000302L	00110111	00101001		
312.	000303L	01010001	00000001		DOPRI KBSC,AC,KBSCNT,1,CO FINISH LIKE REGULAR, BUT INLINE
	000304L	00010010	00110001		
	000305L	00110111	01000100		
313.	000306L	00000111	11110001		LDRT KBSCNT ONLY KEYBOARD INVOLVED (INLINE SRVRTW)
314.					
315.					
316.					. SPECIAL SERVICE REQUESTED INSTRUCTION LEVEL SYSTEM CALL INTERRUPT
317.					. THE P.C. MUST BE BACKED UP IF IMP-NON-ZERO, TO THE IMP SPEC.
318.					. ELSE IT IS POINTING TO THE INSTRUCTION TO EXECUTE NEXT
319.					. OR BEING EXECUTED IF REPEATED.
320.					. NOTE: THE PRESENT WAY CODE WORKS IF NOT REPEATED (OR NOT STARTED YET)
321.					. THEN IMP MUST BE ZERO BECAUSE CAN'T INTERRUPT BETWEEN IMP. SPEC & OPCODE
322.					. BUT CODE BELOW WILL WORK ANYWAY (TOO GENERALIZED)
323.					. I.E. IF IMP-NON-ZERO MUST BE REPEATED THEREFORE MUST BACK IT UP.
324.	000307L	01010001	00000011		DLDMI TEMP,SRSTRT SET RESTART ADDRESS
	000310L	01101111	11110010		
	000311L	01010001	11110000		
	000312L	01101111	11110001		
325.	000313L	11000100	00110100		MWAIT ,MEMPFDL
	000314L	11000111	00100111		
326.	000315L	01011001	11111101		BPGX SCDON
327.	000316L	00110001	11011100		TSTIT ,SWRPT,PSWI IS IT REPEATED?
	000317L	01000101	00100000		
328.	000320L	11000011	00010110		BRA SCDON,TZ NO, THEN P.C. POINTS TO INSTRUCTION
329.	000321L	11001111	00011110		BRA SCLST YES, THEN MAY BACKUP THE PC (TO IMP SPEC)

```

330.
331. >000322L 01011001 11111111
      >000323L 11001111 11111111
332. 000324L 01011001 11111101
      000325L 11001111 00100100
333. 000326L 01011001 11111101
      000327L 11001111 00100010
334.
335. 000330L 00110111 01000001
336. 000331L 00110111 01000101
337. >000332L 01011001 11111111
      >000333L 11001111 11111111
338. 000334L 11111111 11111111
      000335L 11111111 11111111
      000336L 11111111 11111111
      000337L 11111111 11111111
      000340L 11111111 11111111
      000341L 11111111 11111111
      000342L 11111111 11111111
      000343L 11111111 11111111
      000344L 11111111 11111111
      000345L 11111111 11111111
      000346L 11111111 11111111
      000347L 11111111 11111111
      000350L 11111111 11111111
      000351L 11111111 11111111
      000352L 11111111 11111111
      000353L 11111111 11111111
      000354L 11111111 11111111
      000355L 11111111 11111111
      000356L 11111111 11111111
      000357L 11111111 11111111
      000360L 11111111 11111111
      000361L 11111111 11111111
      000362L 11111111 11111111
      000363L 11111111 11111111
      000364L 11111111 11111111
      000365L 11111111 11111111
      000366L 11111111 11111111
      000367L 11111111 11111111
      000370L 11111111 11111111
      000371L 11111111 11111111
      000372L 11111111 11111111
      000373L 11111111 11111111
      000374L 11111111 11111111
      000375L 11111111 11111111
      000376L 11111111 11111111
      000377L 11111111 11111111

```

```

*
DLNLR   BRAX   SRVNXT       DISPLAY SERVICE FINALLY DONE

IVIOL0  BRAX   IVIOL$

UDOP0   BRAX   UDOP

•
MEMPFDL STB     LDMAP       CLEAR INTERRUPT ON ANY MEMORY FAULT
MEMPFCF STB     RDLM        TURN OFF LOAD MODE FOR LODCF MEMORY FAULT
MEMPFO   BRAX   MEMPF$

TABPAGE PROCL

```

```

DLNLR   BPGX   SRVNXT
        TSTIP  ,SUG4K,BSWI
        PAA    SAVNXT,TZ
        LDPI   MAAOH,SYSMH78
        LDPR   STW,LISTICE
        LDPI   MAAOH,SYSCOM78
        LDPR   STW,LISTISE
        BDD    SAVNXT

```

341.								
342.	000400L							
343.								
344.								
345.								
346.								
347.								
348.								
349.								
350.								
351.								
352.								
353.								
354.								
355.	000400L	11001001	00101001		BRA	UDOP0,T@,IZ		157 ALONE IS UNDEFINED
356.	000401L	00110111	00001001		STB	DIMP		CHECK 111
357.	000402L	01010001	01000111		LDPI	URO+URC,PRE		WHATEVER ELSE, C=PRE-RELEASE LEVEL
	000403L	00110111	10000010					
358.	000404L	00110001	11011100		LDTP	PSWI		(ASSUME 1)
359.	000405L	11011001	11101001		BRA	SYSTND,T@,IZ		
360.	000406L	01010001	00000000		TCLR			WILL BE 062 - 022
361.	000407L	11011111	11101001		BRA	SYSTND		
362.								
363.	000410L							
364.								
365.								
366.								
367.								
368.								
369.								
370.								
371.								
372.								
373.	000410L	11011001	11101000		BRA	INFNO,T@,IZ		
374.	000411L	00110111	00001001		STB	DIMP		CHECK IF ITS 1 (111)
375.	000412L	01010001	00000010		LDTI	VER		(ASSUME SO)
376.	000413L	11011000	11110000		BRA	INFEXT,F@,IZ		NO SEE IF 2 OR ABOVE
377.	000414L	00110111	10000000		LDPT	URO+URA		
378.	000415L	01010001	00001100		LDTI	REV		SET PROCESSOR VERSION AND REVISION LEVE
379.	000416L	11011111	11101001		BRA	INFEND		
380.	000417L	00110111	00001001		STB	DIMP		CHECK IF ITS 2 (062)
381.	000420L	01010001	00000000		LDPI	URO+URC,0		
	000421L	00110111	10000010					
382.	000422L	00110111	10000011		LDPT	URO+URD		SET CDE = 0 IN ANY CASE
383.	000423L	00110111	10000100		LDPT	URO+URE		
384.	000424L	11011000	11101001		BRA	INFEND,F@,IZ		WAS IT 062 OR OTHER?
385.	000425L	01010001	00110000		LDTI	CAPABILI		YES, 062 SET CAPABILITIES
386.	000426L							
387.	000426L	00110111	10000001		LDPT	URO+URB		SET B-REGISTER
388.	>000427L	01011001	11111111		INFNO	BRA		AND DONE
	>000430L	11001111	11111111					

*

SYSTAT:

. 8.55 (157) UDOP UNDEFINED OP-CODE
 .
 . 1.30 (111 157) SYSTAT1 PROCESSOR STATUS WORD
 .
 . 1.50 (062 157) SYSTAT2
 . 1.50 (113 157) SYSTAT3 SYSTEM STATUS (UNUSED - 0)
 . 1.50 (174 157) SYSTAT4 C <- 0; B <- 0
 . 1.50 (115 157) SYSTAT5
 . 1.50 (176 157) SYSTAT6 (IF PRE-RELEASE, C <- PRE-RELEASE CODE)
 . 1.50 (117 157) SYSTAT7 (SO CAN TELL PRE-RELEASE LEVEL)
 . 1.50 (022 157) SYSTAT8

*

INFO:

. 0.50 (010) NOP NO-OP (STROBE ON 2200)
 . 1.35 (111 010) INFO A = VERSION #, B = REVISION #
 . 1.90 (062 010) INFO2 B = CAPABILITIES, CDE=0
 . 1.90 (113 010) INFO3 BCDE = 0 (CAPABILITIES)
 . 1.90 (174 010) INFO4 BCDE = 0
 . 1.90 (115 010) INFO5 BCDE = 0
 . 1.90 (176 010) INFO6 BCDE = 0
 . 1.90 (117 010) INFO7 BCDE = 0
 . 1.90 (022 010) INFO8 BCDE = 0

INFEXT

SYSTND

INFEND

INFNO

. LOAD CHARACTER FONT

```

391.
392. 000431L
393.
394.
395.
396.
397.
398. 000431L 00110001 11011100      TSTIP      ,SWUSER,PSWI
      000432L 01000101 00000100
399. 000433L 11000010 00101011      BRA        IVIOLO,FZ
400. 000434L 00110111 01000011      STB        SDLM          PUT IT IN LOAD FONT MODE
401. 000435L 00110001 11010000      DOTIP      ,ND,0177,URI+URA ONLY 7 BITS OF DATA!
      000436L 01010101 01111111
402. 000437L 00010111 10110010
403. 000100
      LODSTEP  EQU        64          ** SET BY HOW MUCH ROOM THERE IS **
      LDCFPT  DOTI      ,SB,LODSTEP  COUNT IN STEPS OF "LODSTEP"
404. 000440L 01010100 01000000      BRA        LDCFNL,TC     IF AT END, DO FINAL STUFF
405. 000441L 11010001 10000001
406.
      LDCFLP  RPT        LODSTEP/2   THERE ARE "LODSTEP" STROBES IN THE SPEEDUP
407.
      STB        SKCH,SKCH
408. 000442L 00110111 01000010      LIST       G
409.
      BRA        LDCFPT,FZ     DONE AND DONE WELL (I HOPE)
410. 000542L 11010010 11011111      STB        SLDCH         DO INITIAL THREE COUNTS
411. 000543L 00110111 00101110      DELAY      2             YAWN - YAWN
412. 000544L 11011111 10011010      STB        RLDCH,SLDCH   END FIRST CHARACTER-SCAN LEVEL STEP
413. 000545L 00110111 00101111
      000546L 00110111 00101110
414. 000547L 01010001 00000111      LDPI       LIMP,7       SET UP FOR 7 ROWS PER FONT
      000550L 00110111 00000001
415. 000551L 00110111 00101111      STB        RLDCH,SLDCH   END THE SECOND AND DO THE THIRD
      000552L 00110111 00101110
416. 000553L 11001110 11111111      DELAY      1             YAWN
417. 000554L 00110001 11100101      LDX        HL2MRH       INIT MARH TO FONT STRING
418. 000555L 00110111 00101111      LDCFLD     STB        RLDCH   RESET FONT LOAD BEFORE CHANGE MAROL
419. 000556L 00110001 11000110      LDX        HL2MRL,SMR   NOW CAN FINALLY START ACTUAL FONT LOAD
      000557L 00110111 01000111
420. 000560L 00110111 00001001      STB        DIMP        LOADING MARL >400 nS AFTER LDCH
421. 000561L 11010100 10001110      MWAIT     ,MEMPCF      IF ERROR, RESET LOAD MODE
      000562L 11000111 00100110
422. 000563L 00110111 00001100      STB        IMAR
423. 000564L 00110001 10000110      LDX        MR2XXL+URL   UPDATE HL THE FASTEST WAY
424. 000565L 00110001 00110110      LDPP      MAROL,MDR,SLDCH GET THE CHARACTER OUT AND LOAD THE FONT
      000566L 00110111 11000000
      000567L 00110111 00101110
425. 000570L 11011000 10010010      BRA        LDCFLD,F@,IZ  LOOP TILL ALL SEVEN ROWS DONE
426. 000571L 00110001 10100101      LDX        MR2XXH+URH   GET NEW HL CAUSE L UPDATED
427. 000572L 00110111 00101111      STB        RLDCH       RESET FONT LOAD
428. 000573L 00110111 01000101      STB        RDLM        RESET LOAD MODE (>400 nS AFTER LDCH)
429. >000574L 01011001 11111111      BRAX      FETCH
      >000575L 11001111 11111111

```

. LOAD CHARACTER FONT

430.
 431. 000576L
 432.
 433.
 434.
 435.
 436. 000576L 01010010 11011100
 437. 000577L 01101111 10110000
 438. 000600L 01010001 00000000
 439. 000601L 11101111 00000000

*

LDCFNL

. FOR THE FINAL STEP ONLY GO PARTIALLY THROUGH THE LOOP

. T >=0=10 STEPS, -1=9 STEPS, -2=8 STEPS, ... -9=1 STEP
 . SKIPS 0 STEPS, 1 STEP 2 STEPS, ... 9 STEPS

DOTA	,AC,LDCFNP+1	ADDS ADDRESS TO NEGATIVE VALUE (CRY SET
BAS	LINK,CC	MOVES FORWARD FROM LDCFNSK (1 TO 9 STEPS
TCLR		MARK ENDED
BRR	LINK	DO AS MANY STEPS AS NEEDED

```

442.
443. 000602L
444.
445.
446. 000602L 00110001 11010011
      000603L 00110111 01001000
447. 000604L 00110001 11011100
      000605L 01000101 00000100
448. 000606L 11000010 00101011
449. 000607L 11011101 01111000
450. 000610L 00110001 11010100
      000611L 00110111 01001001
451. 000612L 00110001 11011111
      000613L 00110111 01001010
452. >000614L 01011001 11111111
      >000615L 11001111 11111111
453.
454. 000616L
455.
456.
457. 000616L 00110111 01000111
458. 000617L 00110001 11011100
      000620L 01010101 00000100
459. 000621L 00110111 01001000
460. 000622L 11000010 00101011
461. 000623L 11011101 01101100
462. 000624L 11010100 01101011
      000625L 11000111 00100101
463. 000626L 00110001 00110110
      000627L 00110111 01001001
464. 000630L 00110001 11011111
      000631L 00110111 01001010
      000632L 00110111 00001100
465. >000633L 01011001 11111111
      >000634L 11001111 11111111
466.
467. 000635L
468.
469.
470. 000635L 00110001 11010011
      000636L 00110111 01001000
471. 000637L 00110001 11011100
      000640L 01000101 00000100
472. 000641L 11000010 00101011
473. 000642L 11011101 01011101
474. 000643L 00110001 11010100
      000644L 00110111 01001001
      000645L 00110111 01011000
475. 000646L 11001110 11111111
476. 000647L 11011101 01011000
477. 000650L 00110001 01011001
      000651L 00110111 10001111
    
```

```

*
DMPOUT:
. 1.65 (IMP 145) DMPOUT (DE) <- (R); ONTO THE DMP BUS
.
LDPP DMPADH,URI+URD SELECT DEVICE
TSTIP ,SWUSER,PSWI
BRA IVIOLO,FZ BUT, MUST BE PRIV'D
BRA $,T@,BR WAIT FOR BUS READY
LDPP DMPADL,URI+URE SELECT ADDRESS/FUNCTION
LDPP DMPDIO,IMPI OUTPUT DATA & PERFORM FUNCTION
BRAX FETCHN

*
DMPSOUT:
. 2.00 (IMP 147) DMPSO PPP (PPP) <- (R); OUTPUT TO DMP BUS
.
STB SMR GET THE ADDRESS LSB
TSTIP ,SWUSER,PSWI,TW
LDPT DMPADH SELECTED MSB ADDRESS IS ZERO
BRA IVIOLO,FZ BUT, MUST BE PRIV'D
BRA $,T@,BR WAIT FOR DEVICE READY TOO
MWAIT ,MEMPF0
LDPP DMPADL,MDR
LDPP DMPDIO,IMPI,IMAR OUTPUT THE DATA & GO FOR NEXT INSTRUCTION
BRAX FETCHN

*
DMPIN:
. 2.00 (IMP 141) DMPIN (R) <- (DE); INPUT FROM THE DMP BUS
.
LDPP DMPADH,URI+URD SELECT DESIRED DEVICE
TSTIP ,SWUSER,PSWI
BRA IVIOLO,FZ ONLY IF ALLOWED TO
BRA $,T@,BR AND WAIT FOR IT TO BE READY
LDPP DMPADL,URI+URE,DMPRDS SELECT ADDRESS/FUNCTION TO BE INPUT
NOOP
BRA $,T@,BR
LDPP IMPO,DMPDIO FINALLY GET THE DATA
    
```

```

478. >000652L 01011001 11111111
      >000653L 11001111 11111111
479.
480. 000654L
481.
482.
483. 000654L 00110111 01000111
484. 000655L 00110001 11011100
      000656L 01010101 00000100
485. 000657L 00110111 01001000
486. 000660L 11000010 00101011
487. 000661L 11011101 01001110
488. 000662L 11010100 01001101
      000663L 11000111 00100101
489. 000664L 00110001 00110110
      000665L 00110111 01001001
      000666L 00110111 01011000
490. 000667L 11001110 11111111
491. 000670L 11011101 01000111
492. 000671L 00110001 01011001
      000672L 00110111 10001111
493. >000673L 01011001 11111111
      >000674L 11001111 11111111
494.
495. 000675L
496.
497.
498.
499.
500.
501. 000675L 00110001 11000110
      000676L 00110001 11100101
502. 000677L 00110001 11010011
      000700L 00110111 01001000
503. 000701L 00110111 01000111
504. 000702L 00110001 11011100
      000703L 01000101 00000100
505. 000704L 11000010 00101011
506. 000705L 11011101 00111010
507. 000706L 00110001 11010100
      000707L 00110111 01001001
508. 000710L 11010100 00110111
      000711L 11000111 00100101
509. 000712L 00110001 00110110
      000713L 00110111 01001010
510. 000714L 01101111 11110001
511. 000715L
512.
513. 000715L 00110111 00001100
514. 000716L 00110001 10000110
      000717L 00110001 10100101
515. 000720L 00110001 11000100
    
```

```

BRAX    FETCHN

*
DMPSIN:
. 2.20  (IMP 143)  DMPSIN PPP      (R) <- (PPP); FROM DMP BUS
.
      STB    SMR      GET THE PORT ADDRESS
      TSTIP  ,SWUSER,PSWI,TW
      LDPT   DMPADH   ZERO TO MSB ADDRESS
      BRA    IVIOLO,FZ ONLY IF ALLOWED TO
      BRA    $,T@,BR  AND WAIT FOR IT TO BE READY
      MWAIT  ,MEMPFO

      LDPP   DMPADL,MDR,DMPRDS  SELECT ADDRESS/FUNCTION TO BE INPUT

      NOOP
      BRA    $,T@,BR
      LDPP   IMPO,DMPDTI      FINALLY GET THE DATA

BRAX    FETCHN

*
BLKOUT:
.      ( 173)  BLKOUT      T <- (DE) <- (HL); OUTPUT TO DMP BUS
.                                     DE <+ 1; HL <+ 1; C <- C - 1
.                                     UNTIL (T + B = 0400) OR (C = 0)
. 0.10 + 5.05 * C - 0.6 IF MATCH

      DLDX   HL2MR      GET DATA TO OUTPUT

      LDPP   DMPADH,URI+URD  SELECT DEVICE TO OUTPUT IT TO

      STB    SMR
      TSTIP  ,SWUSER,PSWI

      BRA    IVIOLO,FZ   ONLY IF PRIV'D
      BRA    $,T@,BR    WAIT FOR BUS READY
      LDPP   DMPADL,URI+URE  FINISH ADDRESS SELECT

      MWAIT  ,MEMPFO

      LDPP   DMPDIO,MDR    OUTPUT THE DATA & SAVE IT TOO

      LDRT   TEMP1

BLKLOOP
. 2.95 (RPT), 2.45 (MATCH), 3.05 (END)
      STB    IMAR
      DLDX   MR2HL      UPDATE HL & DE ADDRESS POINTERS

      DLDX   DE2MR,,IMAR
    
```


. DMP I/O INTERFACE INSTRUCTIONS

000721L	00110001	11100011			
000722L	00110111	00001100			
516.	000723L	00110001	10000100	DLDX	MR2DE
	000724L	00110001	10100011		
517.	000725L	00110001	11010001	TSTRP	AC,TEMP1,URI+URB,CO TEST B-COMPLETION
	000726L	01110010	00000001		
518.	000727L	11010000	00100101	BRA	BLKGO,FC
519.	000730L	11010011	00011011	BRA	BLKEND,TZ
520.	000731L	00010111	10110010	CCLR	
521.	000732L	00110001	11010010	BLKGO	DOPIP URO+URC,SB,1,URI+URC COUNT DOWN IN C
	000733L	01010100	00000001		
	000734L	00110111	10000010		
522.	000735L	11010011	00011011	BRA	BLKEND,TZ
523.	000736L	00110001	00110000	TSTPT	FI,SRVREQ CAN WE REPEAT QUICKLY?
524.	000737L	11010010	00011101	BRA	BLKRPT,FZ NO
525.	000740L	00111001	00110100	BRPX	IDCOD YES
	000741L	10101111	00110011		
526.	>000742L	01011001	11111111	BLKRPT	BRAX SRVRPT DO SERVICE AS NEEDED
	>000743L	11001111	11111111		
527.	000744L	00110001	11011100	BLKEND	DOPIP PSWQ,ND,-1-SWRPT,PSWI
	000745L	01010101	11011111		
	000746L	00110111	10001100		
528.	>000747L	01011001	11111111	BRAX	FETCH
	>000750L	11001111	11111111		
529.					
530.	000751L				
531.					
532.					
533.					
534.					
535.					
536.	000751L	00110001	11010011	LDPP	DMPADH,URI+URD SELECT DEVICE
	000752L	00110111	01001000		
537.	000753L	00110001	11011100	TSTIP	,SWUSER,PSWI
	000754L	01000101	00000100		
538.	000755L	11000010	00101011	BRA	IVIOL0,FZ CONTINUE ONLY IF PRIV'D
539.	000756L	11011101	00010001	BRA	\$,T@,BR
540.	000757L	00110001	11010100	LDPP	DMPADL,URI+URE,DMPRDS SELECT ADDRESS/FUNCTION AND READ
	000760L	00110111	01001001		
	000761L	00110111	01011000		
541.	000762L	00110001	11000110	DLDX	HL2MR
	000763L	00110001	11100101		
542.	000764L	11011101	00001011	BRA	\$,T@,BR
543.	000765L	00110001	01011001	LDPP	MDW,DMPDTI GET THAT DATA & WRITE IT TO MEMORY
	000766L	00110111	00101001		
544.	000767L	01101111	11110001	LDRT	TEMP1
545.	000770L	11010100	00000111	MWAIT	,MEMPF0 WAIT FOR COMPLETION
	000771L	11000111	00100101		
546.	000772L	11011111	00110010	BRA	BLKLOOP
547.	000773L	11111111	11111111	TABPAGE	PROCL
	000774L	11111111	11111111		
	000775L	11111111	11111111		

*

BLKIN:

(177) BLKIN T ← (HL) ← (DE); FROM DMP BUS
 HL ←+ 1; DE ←+ 1; C ←-- 1
 UNTIL (T + B = 0400) OR (C = 0)
 . 0.10 + 5.75 * C - 0.60 IF MATCH

000776L 11111111 11111111
000777L 11111111 11111111

. INPUT OUTPUT OPERATIONS

```

550.
551. 001000L
552.
553.
554.
555.
556. 001000L 00110001 11011100
      001001L 01000101 00000100
557. 001002L 11000010 00100100
558. 001003L 01000101 00001000
559. 001004L 11000010 11110011
560. 001005L 01010001 00000110
561. 001006L 11001111 00100001
562.
563. 001007L
564.
565.
566.
567.
568. 001007L 00110001 11011100
      001010L 01000101 00000100
569. 001011L 11000010 00100100
570. 001012L 01000101 00001000
571. 001013L 11000011 11101001
572. 001014L 01000101 00010000
573. 001015L 11000011 11101101
574. 001016L 00110001 01010010
      001017L 00110111 10001111
575. >001020L 01011001 11111111
      >001021L 11001111 11111111
576.
577. 001022L 00110001 01010011
      001023L 00110111 10001111
578. >001024L 01011001 11111111
      >001025L 11001111 11111111
579.
580. 001026L 01010001 00000000
      001027L 00110111 10001111
581. >001030L 01011001 11111111
      >001031L 11001111 11111111

```

*
PIN:
. (103) PIN PARITY CHECKING INPUT
. (IMP 103) PINR (R) <- INBUS; PARITY CHECK
. 1.45 (DATA); 1.55 (STATUS); 1.30 (NON-RIM)
TSTIP ,SWUSER,PSWI CONTINUE ONLY IN PRIV'D MODE
BRA IVIOL\$,FZ
TSTIT ,SWIRIM ONLY OPERATE IF RIM DEFINED
BRA INPRIM,FZ
PFMIN LDTI SVINP PIN OR MIN TO NON RIM IS PARITY FAULT
BRA SCLSTW
*
INPUT:
. (101) IN INPUT FROM 5500 BUS
. (IMP 101) INR (R) <- INBUS
. 1.35 (DATA); 1.45 (STATUS); 1.20 (NON-RIM)
TSTIP ,SWUSER,PSWI CONTINUE ONLY IN PRIV'D MODE
BRA IVIOL\$,FZ
TSTIT ,SWIRIM ONLY OPERATE IF RIM DEFINED
BRA INPZRO,TZ
INPRIM TSTIT ,SWSTDT WANT STATUS OR DATA?
BRA INSTAT,TZ
LDPP IMPO,RIMDATI GET RIM DATA
BRAX FETCHN
INSTAT LDPP IMPO,RIMSTAI GET RIM STATUS
BRAX FETCHN
INPZRO LDPI IMPO,0 GET DATA OF ZERO - THERE IS NO I/O BUS!
BRAX FETCHN

INPUT OUTPUT OPERATIONS

```

582.
583. 001032L
584.
585.
586.
587.
588. 001032L 00110001 11011100
      001033L 01000101 00000100
589. 001034L 11000010 00100100
590. 001035L 01010101 11101111
      001036L 00110111 10001100
591. 001037L 01010001 10101010
      001040L 00110111 11000000
      001041L 01010001 11101111
      001042L 00110111 11100000
592. 001043L 00110001 11011111
      001044L 00110111 00101001
593. 001045L 01000000 10011100
594. 001046L 11000010 11010110
595. 001047L 01010001 00001000
596. 001050L 11001111 11000111
597.
598. 001051L 01010001 11110111
599. 001052L 11001111 11010000
600.
601. 001053L
602.
603.
604.
605. 001053L 00110001 11011100
      001054L 01000101 00000100
606. 001055L 11000010 00100100
607. 001056L 01010001 11101111
608. 001057L 00110101 11011100
      001060L 00110111 10001100
609. 001061L 00110111 00000100
610. >001062L 01011001 11111111
      >001063L 11001111 11111111
611.
612. 001064L
613.
614.
615.
616. 001064L 00110001 11011100
      001065L 01000101 00000100
617. 001066L 11000010 00100100
618. 001067L 01010001 00010000
619. 001070L 00110011 11011100
      001071L 00110111 10001100
620. >001072L 01011001 11111111
      >001073L 11001111 11111111

```

```

+
EXADR:
. ( 121) EX ADR          SELECT DEVICE (AND PUT IN STATUS MODE)
. (IMP 121) EX ADR      (SEXADR) <- OUTBUS <- (R)
. 2.50 (RIM); 2.75 (NON-RIM)

TSTIP ,SWUSER,PSWI      SHOULD I HAVE DONE THAT?

BRA   IVIOLs,FZ
DOPI  PSWO,ND,-1-SWSTDT MARK IN STATUS MODE

DLDPI MARO,SEXADR

LDPP  MDW,IMPI          OUTPUT ADDRESS TO ITS SAVE AREA

TSTIT XR,RIMADR        IS THE RIM BEING ADDRESSED?
BRA   ADRNON,FZ
LDTI  SWIRIM           YES, MARK AS ADDRESSED
BRA   PSWOR

ADRNON LDTI -1-SWIRIM   NO, CLEAR MARKINGS
BRA   PSWND

*
EXSTAT:
. 1.20 ( 123) EX STATUS  PUT IN STATUS MODE
. 1.20 (IMP 123) EX STATUS OUTBUS <- (R)

TSTIP ,SWUSER,PSWI      SHOULD I HAVE DONE THAT?

BRA   IVIOLs,FZ
LDTI  -1-SWSTDT        CLEAR STATUS (SET DATA) MODE
PSWND DOPP  PSWO,ND,PSWI MARK IN STATUS MODE

LDPT  MODW
BRAX  FETCHWS          ** FETCHW FOR EX ADR ONLY **

*
EXDATA:
. 1.05 ( 125) EX DATA   PUT IN DATA MODE
. 1.05 (IMP 125) EX DATA OUTBUS <- (R)

TSTIP ,SWUSER,PSWI      SHOULD I HAVE DONE THAT?

COM4X LDTI IVIOLs,FZ    MARK IN DATA MODE
PSWOR DOPP  PSWO,OR,PSWI

BRAX  FETCHWS          ** FETCHW FOR EX ADR ONLY **

```

TSTIT 15w64K
BRA
LDPR STUSSTIGE

621.					
622.	001074L				
623.					
624.					
625.					
626.					
627.	001074L	00110001	11011100	TSTIP	,SWUSER,PSWI
		001075L	01000101		
628.	001076L	11000010	00100100	BRA	IVIOLS,FZ
629.	001077L	01000101	00001000	TSTIT	,SWIRIM
630.	001100L	11000011	10101111	BRA	IRIMF,TZ
631.	001101L	00110001	11011111	LDPP	RIMDATO,IMPI
		001102L	00110111		
632.	>001103L	01011001	11111111	BRAX	FETCHN
	>001104L	11001111	11111111		
633.					
634.	001105L				
635.					
636.					
637.					
638.					
639.	001105L	00110001	11011100	TSTIP	,SWUSER,PSWI
		001106L	01000101		
640.	001107L	11000010	00100100	BRA	IVIOLS,FZ
641.	001110L	01000101	00001000	TSTIT	,SWIRIM
642.	001111L	11000011	10101111	BRA	IRIMF,TZ
643.	001112L	00110001	11011111	LDPP	RIMADRO,IMPI
		001113L	00110111		
644.	001114L	11001111	11001000	BRA	COM4X
645.					
646.	001115L				
647.					
648.					
649.					
650.					
651.					
652.					
653.					
654.					
655.					
656.	001115L	00110001	11011100	TSTIP	,SWUSER,PSWI
		001116L	01000101		
657.	001117L	11000010	00100100	BRA	IVIOLS,FZ
658.	>001120L	01011001	11111111	IRIMF	
	>001121L	11001111	11111111	BRAX	FETCHN

```

*
EXWRITE:
. ( 127) EX WRITE      WRITE DATA TO THE DEVICE
. (IMP 127) EXr WRITE
. 1.15 (RIM); 0.95 (NON-RIM)

*
EXCOM4:
. ( 137) EX COM4      DO CONTROL STROBE 4
. (IMP 137) EXr COM4
. 1.75 (RIM); 0.95 (NON-RIM)

*
OUTPUT:
. 0.65 (1xy: x=2,3: y ODD) EX COM OUTPUT TO 5500 BUS
. 0.65 (IMP 1xy) EXr COM  OUTBUS <- (R)

. (IMP 133) EXr COM2    ** NO-OP **
. ( 133) EX COM2      DO CONTROL STROBE 2

. ( 135) EX COM3      DO CONTROL STROBE 3
. (IMP 135) EXr COM3  ** NO-OP **

*
TSTIP ,SWUSER,PSWI

IRIMF  BRA IVIOLS,FZ  ONLY CONTINUE IF PRIVED
        BRAX  FETCHN  ELSE IT IS A NO-OP
    
```

. INPUT OUTPUT OPERATIONS

```

659.
660. 001122L
661.
662.
663.
664.
665. 001122L 00110001 11011100          TSTIP      ,SWUSER,PSWI
      001123L 01000101 00000100
666. 001124L 11000010 00100100          BRA        IVIOL$,FZ          ONLY CONTINUE IF PRIVED
667. 001125L 01000101 00001000          TSTIT     ,SWIRIM
668. 001126L 11000011 10010100          BRA        EXCOMJ,TZ
669. 001127L 00110001 11011111          LDTP      IMPI                GET DATA TO BE STROBED TO THE RIM
670. 001130L 00010111 10100010          SHIFT     SL,CC
671. 001131L 01010101 00001110          DOTI      ,ND,07<1          SELECT LOWER 3 BITS (SHIFTED UP ONE)
672. 001132L 01010010 10010100          DORA      LINK,AC,EXCOMJ     ADDRESS INTO FUNCTION TABLE
      001133L 01101111 11110000
673. 001134L 11101111 00000000          BRR       LINK                AND GO DO IT!
674.
675. 001135L 00110111 01010001          STB       EXCOM17           7 (1.85) RESET CONFIG
676. 001136L 11001110 11111111          NOOP
677. >001137L 01011001 11111111          BRAX      FETCHN           6 (1.60) NO POR ANY MORE
      >001140L 11001111 11111111
678. 001141L 01010001 10001001          BRC       XBUF$,XC15       5 (2.95) SET BUFFER PNTR FOR RCVR
      001142L 11001111 10010010
679. 001143L 01010001 10001100          BRC       XBUF$,XC14       4 (2.95) SET BUFFER PNTR FOR XMTR
      001144L 11001111 10010010
680. 001145L 01010001 10010100          BRC       XBUF$,EXCOMJ     3 (2.80) SET BUFFER PNTR FOR PROCESSOR
      001146L 11001111 10010010
681. 001147L 00110111 01010101          STB       EXCOM12           2 (1.95) DISABLE RECEIVER
682. 001150L 11001111 10010100          BRA        EXCOMJ
683. 001151L 00110111 01010100          STB       EXCOM11           1 (1.85) DISABLE TRANSMITTER
684. 001152L 11001110 11111111          NOOP
685. 001153L
      FTCHIAB
686. >001153L 01011001 11111111          EXCOMJ    BRAX      FETCHN           0 (1.60) NO IPE (TO BE CLEARED) ANY MORE
      >001154L 11001111 11111111
687.
688. 001155L 01101111 11110000          XBUF$     BAS        LINK
689. 001156L 00110001 10001001          LDX       MR2PCL
690. 001157L 00110001 11001111          LDX       IM2MRL,LDRIMBP    DON'T LOSE UPDATED PC
      001160L 00110111 00101101          LOAD BUFFER POINTER TO THE RIM
691. 001161L 00110001 11001001          LDX       PC2MRL           RESTORE PC
692. 001162L 11101111 00000000          BRR       LINK                NOW DO OPERATION (IF NEEDED)
693.
694. 001163L 00110111 01010110          XC14      STB        EXCOM14       BUFFER SELECTED, START TRANSMITTER
695. >001164L 01011001 11111111          BRAX      FETCHN
      >001165L 11001111 11111111
696.
697. 001166L 00110111 01010111          XC15      STB        EXCOM15       BUFFER SELECTED, START RECEIVER
698. >001167L 01011001 11111111          BRAX      FETCHN
      >001170L 11001111 11111111
    
```

```

699.
700. 001171L
701.
702.
703.
704.
705. 001171L 00110001 11100101      DLRX      HL2MR      PRELOAD MAR WITH WHERE TO SAVE DATA
      001172L 00110001 11000110
706. 001173L 00110001 11011100      TSTIP     ,SWUSER,PSWI
      001174L 01000101 00000100
707. 001175L 11000010 00100100      BRA      !VIOL$,FZ      ONLY CONTINUE IF PRIVED
708. 001176L 01000101 00001000      TSTIT    ,SWIRIM
709. 001177L 11000011 11111010      BRA      PFMIN,TZ      IF NOT RIM THEN PARITY FAULT
710. 001200L 01000101 00010000      TSTIT    ,SWSTDT      IF STATUS MODE THEN DO STATUS MIN??
711. 001201L 11000011 01110000      BRA      MINST,TZ
712. 001202L
713. 001202L 00110001 01010010      MINDT    LDPP      MDW,RIMDATI      ** LOOP IS 1.60 MICRO-SECONDS!!!
      001203L 00110111 00101001      GET RIM DATA & WRITE TO MEMORY
714. 001204L 00110001 00110000      LDTP     SRVREQ      ** DELAY 150 NS **
715. 001205L 00010111 10110010      CCLR
716. 001206L 00110001 11010010      DOPIP    URFO+URC,SB,1,URI+URC  DECREMENT COUNT IN C
      001207L 01010100 00000001
      001210L 00110111 01100010
717. 001211L 11000100 01110110      MWAIT    ,MEMPF1      WAIT FOR MEMORY OP
      001212L 11010111 00010001
718. 001213L 00110111 00001100      STB      IMAR
719. 001214L 01000101 00001111      TSTIT    ,017      AT THE END?
720. 001215L 11000010 01111101      BRA      MINDT,FZ
721. 001216L 11011111 00001111      BRA      MIOEND      YES
722.
723. 001217L
724. 001217L 00110001 01010011      MINST    LDPP      MDW,RIMSTAI      GET RIM STATUS & WRITE TO MEMORY
      001220L 00110111 00101001
725. 001221L 00110001 00110000      LDTP     SRVREQ      ** DELAY 150 NS **
726. 001222L 00010111 10110010      CCLR
727. 001223L 00110001 11010010      DOPIP    URFO+URC,SB,1,URI+URC  DECREMENT COUNT IN C
      001224L 01010100 00000001
      001225L 00110111 01100010
728. 001226L 11000100 01101001      MWAIT    ,MEMPF1      WAIT FOR MEMORY OP
      001227L 11010111 00010001
729. 001230L 00110111 00001100      STB      IMAR
730. 001231L 01000101 00001111      TSTIT    ,017      AT THE END?
731. 001232L 11000010 01110000      BRA      MINST,FZ
732. 001233L 11011111 00001111      BRA      MIOEND      YES
    
```

```

733.
734. 001234L
735.
736.
737.
738.
739. 001234L 00110001 11000110      DLDX      HL2MR      GET DATA AS SOON AS POSSIBLE
      001235L 00110001 11100101
740. 001236L 00110001 11011100      TSTIP     ,SWUSER,PSWI  ONLY CONTINUE IF PRIVED
      001237L 01000101 00000100
741. 001240L 11000010 00100100      BRA       IVIOL$,FZ
742. 001241L 00110111 01000111      STB       SMR
743. 001242L 01000101 00001000      TSTIT     ,SWIRIM
744. 001243L 11000010 01000111      BRA       MOUTOUT,FZ      DO MOUT OR DO NOTHING
745.
746. 001244L 00110001 11010010      DOTIP     ,ND,017,URI+URC  UPDATE HL & C FOR MOUT
      001245L 01010101 00001111
747. 001246L 11000010 01010111      BRA       MOUTN16,FZ      TO NON-EXISTANT DEVICE
748. 001247L 01010001 00010000      LDTI     16              IF C IS ZERO, USE 16
749. 001250L 01101111 11110001      LDRT     TEMPI
750. 001251L 00110001 11010010      DOPRP    URFO+URC,SB,TEMPI,URI+URC,C0  COUNT DOWN C
      001252L 01110100 00110001
      001253L 00110111 01100010
751. 001254L 00110001 11010110      DQPRP    URO+URL,SB,TEMPI,URI+URL,C0  COUNT DOWN HL
      001255L 01110100 00110001
      001256L 00110111 10000110
752. >001257L 01011001 11111111      BRAX     FETCHW,FC      (NO CARRY TO H)
      >001260L 11000000 11111111
753. 001261L 00110001 11010101      DQPIP    URO+URH,SB,0,URI+URH  COUNT DOWN HL
      001262L 01010100 00000000
      001263L 00110111 10000101
754. >001264L 11001111 11111111      BRA       FETCHW      (FETCHW FOR THE WASTED SMR!)
755.
756. 001265L      MOUTLP      ** LOOP IS 1.60 MICRO-SECONDS!!!
757. 001265L 00110111 01000111      STB       SMR
758. 001266L 00110001 00110110      LDPP     RIMDATO,MDR      GET DATA OUT TO THE RIM
      001267L 00110111 00101000
759. 001270L 00010111 10110010      MOUTOUT  CCLR
760. 001271L 00110001 11010010      DQPIP    URFO+URC,SB,1,URI+URC  DECREMENT THE COUNT IN C
      001272L 01010100 00000001
      001273L 00110111 01100010
761. 001274L 11000100 01000011      MWAIT    ,MEMPF1
      001275L 11010111 00010001
762. 001276L 00110111 00001100      STB       IMAR
763. 001277L 01000101 00001111      TSTIT     ,017      BASE 16 END?
764. 001300L 11000010 01001010      BRA       MOUTLP,FZ      COMPLETED BASE 16 IF JUMP
765.      RPT       3          ** DELAY 300 NS (FOR 1.60 TOTAL) **
766. 001301L 11001110 11111111      NOOP
766. 001302L 11001110 11111111      NOOP      AND KEEP CODE THE SAME SIZE
766. 001303L 11001110 11111111      NOOP      AND KEEP CODE THE SAME SIZE
767. 001304L 00110001 00110110      LDPP     RIMDATO,MDR      GET FINAL DATA OUT TO THE RIM
      001305L 00110111 00101000
    
```


768. 001306L 11011111 00001111

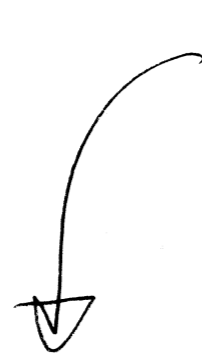
BRA MIOEND

771.
 772.
 773.
 774. 001307L
 775.
 776. 001307L 01101111 11110010
 777. 001310L 01010001 11110000
 778. 001311L 11001111 00101100
 779.
 780. 001312L
 781.
 782.
 783.
 784.
 785. 001312L 01010001 00110000
 786. 001313L 11001111 00110010
 787.
 788. 001314L
 789.
 790.
 791.
 792.
 793. 001314L 01010001 00101010
 794.
 795.
 796. 001315L
 797.
 798.
 799. 001315L 01101111 11110010
 800. 001316L 01010001 11101111
 001317L 01101111 11110001
 801. 001320L 11001111 00011000
 802.
 803. 001321L
 804.
 805. 001321L 01101111 11110010
 806. 001322L 01010001 11101111
 807. 001323L 01101111 11110001
 808. 001324L 00110001 11001001
 001325L 00110001 11101000
 001326L 00110111 00001100
 809. 001327L 11001111 00011000

*
 . NOTE: FOR ALL SYSTEM CALLS, THE WAY THE PC SHOULD BE LEFT IS SPECIFIED
 *
 SCROMLI: !! UP THE PC TO NEXT INSTRUCTION
 . 8.70 !! MEMORY OR SECTOR TABLE PARITY ERROR
 ROM VECTOR SAVED
 HOPEFULLY POINTING AT THE NEXT INSTRUCTION
 LDRT TEMPL
 LDTI SYSROM>8
 BRA SCROMX
 *
 BP: !! PC LEFT AFTER THE INSTRUCTION
 (052) BP BREAKPOINT
 . 8.35 (SP-2 | SP-1) <- PC
 . SP <- SP - 2; PC <- BRKPNT
 LDTI SVBKPNT
 BRA SCBP
 *
 SC: !! PC LEFT AFTER THE INSTRUCTION
 (067) SC SYSTEM CALL (SUPERVISOR CALL)
 . 8.15 (SP-2 | SP-1) <- PC
 . SP <- SP - 2; PC <- SYSCAL
 LDTI SVSCAL
 BRA SCBP
 *
 SCBP !! UP THE PC TO NEXT INSTRUCTION
 . 8.05 !! RAM VECTOR FOR INTERRUPT
 LDRT TEMPL
 LDRI TEMPH, SYSIVR>8
 BRA SCPC
 *
 SCRAMI: !! PC LEFT AFTER THE INSTRUCTION
 . 8.50 !! MEMORY ACCESS & WRITE VIOLATIONS
 LDRT TEMPL
 LDTI SYSIVR>8
 SCROMX LDRT TEMPH
 DLDX PC2MR,,IMAR
 BRA SCPC
 GO TO THE RAM VECTOR

LDPT NAKON, SDN

810.								
811.	001330L			UDPOP:		!! PC LEFT AT NEXT INSTRUCTION		
812.				.	(000) HALT	UNDEFINED PRIVILEGED OP		
813.				.	(001) HALT	(SP-1 SP-1) <- PC		
814.				.	(377) HALT	SP <- SP - 2; PC <- IVIOL		
815.				.	8.50 (+0.10 IF NOT USER MODE)			
816.								
817.	001330L	00110001	11011100		TSTIP	,SWUSER,PSWI		
	001331L	01000101	00000100					
818.	001332L	11000011	00100010		BRA	UDOP,TZ	UNDEFINED IF IN PRIV MODE	
819.				*				
820.	001333L	01010001	00011110	IVIOLs:	LDTI	SVIVIOL	!! PC LEFT AT LAST INSTRUCTION	
821.	001334L	11001111	00100001		BRA	SCLSTW	TRIES PRIV'D INSTRUCTION WHILE USER MOD	
822.				*				
823.	001335L			UDOP:		!! PC LEFT AT LAST INSTRUCTION		
824.				.	8.05 (171)	(SP-2 SP-1) <- PC		
825.				.	8.05 (175)	SP <- SP - 2; PC <- UAINST		
826.								
827.	001335L	01010001	00110110		LDTI	SVUAINS	UNDEFINED OP-CODE VECTOR SYSCALL	
828.				*				
829.	001336L			SCLSTW		!! RAM VECTOR INTERRUPT		
830.				.	7.95	!! 5500 I/O BUS PARITY ERROR		
831.				.		!! BACKUP PC TO START OF		
832.				.		!! INTERRUPTING INSTRUCTION		
833.								
834.	001336L	11000100	00100001		MWAIT	,\$+1		
	001337L	11000111	00011111					
835.	001340L	01101111	11110010		LDRT	TEMPL	SAVE RAM VECTOR ADDRESS	
836.	001341L	01010001	11101111	SCLST:	LDRI	TEMPH,SYIVR>8		
	001342L	01101111	11110001					
837.				.	7.65 (+ 0.65 IF IMP # 0)			
838.	001343L	11001001	00010110		BRA	SCDON,T@,IZ	POINTS TO START OF LAST INSTRUCTION.	
839.				.			!! 1 MSEC INTERRUPT WHEN REPEATED	
840.	001344L	00110001	11001001		DLDX	PC2MR,,DMAR	BACK UP TO IMP SPEC CODE	
	001345L	00110001	11101000					
	001346L	00110111	00001101					
841.	001347L	00110001	10001001	SCPC	DLDX	MR2PC	!! SYSTEM CALL PERFORM SECTION	
	001350L	00110001	10101000					
842.				.	7.55	SAVE P.C. AS SHOULD BE		
843.				*				
844.	001351L			SCDON:		!! 1 MSEC INTERRUPT WHEN NOT REPEATED		
845.				.	7.25			
846.								
847.	001351L	01010001	11110000		LDPI	MAR0H,SYSPROM>8.AND.0360	CORRECT ENTRY 017 TO BE SURE	
	001352L	00110111	11100000					
848.	001353L	00110111	00000101		LDPT	STW	IN THE SECTOR TABLE	
849.	001354L	01010001	11000000		LDTI	0300		
850.	001355L	00110101	11001011		DOP	SP2MRL,ND	POINT TO THE PSW SAVE BYTE	
851.	001356L	00110001	11101010		LDX	SP2MRH,DMAR		
	001357L	00110111	00001101					
852.	001360L	00110001	11011100		DOPIP	MODW,ND,-1-SWSCF,PSWI	CLEAR NECESSARY SYSCALL FLAGS	
	001361L	01010101	11011010		TSTIT			



LDPI MAR0H,SYSPROM>8.AND.0360 CORRECT ENTRY 017 TO BE SURE
LDPT STW IN THE SECTOR TABLE
LDTI 0300
DOP SP2MRL,ND POINT TO THE PSW SAVE BYTE
LDX SP2MRH,DMAR
DOPIP MODW,ND,-1-SWSCF,PSWI CLEAR NECESSARY SYSCALL FLAGS
TSTIT
LDPP MODW,PSWI
DAA SC D 64K

. SYSTEM CALLS AND OP-CODES FOR IT

853.	001362L	00110111	00000100				
	001363L	00110001	11011100	LDPP	MDW,PSWI	SAVE ORIGINAL PSW IN ITS SAVE AREA	
	001364L	00110111	00101001				
854.	001365L	01010101	11011010	DOPI	PSWO,ND,-1-SWSCF	SET NEW SYSCALL FLAGS	
	001366L	00110111	10001100				
855.	001367L	01010001	00001001	LDPI	LIMP,PCL	GET SET FOR PUSH OF THE P.C.	
	001370L	00110111	00000001				
856.	001371L	11000100	00000110	MWAIT	,IGNORE	WAIT ON WRITE & IF ERROR, TROUBLE	
857.	>001372L	01011001	11111111	BRCX	PSHSTO,FO,MP,PCMOD	IF NO ERROR, GO TO IT (SAVED 1 WORD)	
	>001373L	01010001	11111111				
	>001374L	11000110	11111111				
858.							
859.							
860.							
861.							
862.							
863.	001375L	01010001	00000110	LDTI	SRSYSMF	DO SPECIAL INTERRUPT	
864.	001376L	01011001	11111111	BRAX	FETPC	FORGET PUSH, WILL PROBABLY NOT WORK	
	001377L	11001111	11011011				
865.							
866.							

SCDNORM LDPI MAROH, SYSRCD = 8, STW

SCD64K

SCSTKP

*
 .MEMPFSC
 . WOW! SYSTEM SAVE AREA HAD SECTOR TABLE OR WRITE PROTECT FAULT
 . USE THE ROM VECTOR POINT TO MARK A DOUBLE BAD INTERRUPT

SCSTKP
 WAIT, TDT
 TSTIP, SW 64K, PSWI
 BVA SC 2 PCT, T2
 MWAIT, MEMPFSC
 DCTIP, ND, \$200, SPIL
 DOPI MAROH, OR, SE SAV SP, AND, \$177
 LDPP MDW, SPIL
 NOOP
 SC 2 PCT -> MWAIT
 BRAX PCMOD

. REGL, ALPHA, BETA MODE SWAPS AND SUB-PARTS

```

869.
870. 001400L
871.
872.
873.
874.
875.
876.
877.
878.
879.
880.
881.
882.
883.
884. 001400L 00110001 11011100      TSTIP      ,SWUSER,PSWI      ONLY IF PRIV'D
      001401L 01000101 00000100
885. 001402L 11000010 00100100      BRA        ,IVIO$,FZ
886. 001403L 01000101 00100000      TSTIT      ,SWRPT
887. 001404L 11010010 11000110      BRA        BETAL,FZ      IF REPEATED DO SECOND HALF
888. 001405L 11011011 11000110      BRA        BETAL,T@,IO    IF ODD, ONLY LOAD BETA REGS
889. 001406L 01000101 10000000      TSTIT      ,SWALBT      TEST HERE, SYSSAV NEEDS IT
890. 001407L 11011000 11110010      BRA        SYSSAV,F@,IZ   SYSTEM SAVE IF NON-ZERO
891. 001410L 11000010 10010100      BRA        FTCHIAB,FZ    SIMPLE BETA, FORGET IT, ALREADY IN BETA
892. 001411L 01010011 00100000      DOPI       PSWO,OR,SWRPT     TWO PARTS, SO REPEATED
      001412L 00110111 10001100
893. 001413L 01010001 00111110      ALPHAS     LDTI       SESAVAF.AND.0177  POINT TO CORRECT SAVE AREA (7 BITS!)
894. 001414L 11011111 11100100      BRA        MODSAV
895.
896. 001415L
897.
898.
899.
900. 001415L 11010011 11110100      BRA        ALPHAS,TZ     SAVE ALL REGISTERS TO THE ALPHA SET
901. 001416L 11011111 11100101      BRA        BETAS        NO, TO BETA SET

```

*
BETA:
. (020) BETA SAVE ALPHA REGS AND LOAD BETA SET
. 27.90 (1.35 IN BETA) 'FXLHEDCBA' <- FXLHEDCBA
. FXLHEDCBA <- "FXLHEDCBA"
. (111 020) BETAL LOAD REGS FROM BETA SAVE AREA
. 13.45 FXLHEDCBA <- "FXLHEDCBA"
. (062 020) SYSSAV SAVE SYSTEM REGS
. 14.00 "'FXLHEDCBA"' <- FXLHEDCBA
. NOTE: CAN NOT IMS. INTERRUPT BETWEEN BETA & FOLLOWING INSTRUCTION.

```

902.
903. 001417L
904.
905.
906.
907.
908.
909.
910.
911.
912.
913.
914.
915.
916.
917.
918. 001417L 00110001 11011100
      001420L 01000101 00000100
919. 001421L 11000010 00100100
920. 001422L 01000101 00100000
921. 001423L 11010010 10011100
922. 001424L 11011011 10011100
923. 001425L 11011000 10111000
924. 001426L 01000101 10000000
925. 001427L 11000011 10010100
926. 001430L 01010011 00100000
      001431L 00110111 10001100
927. 001432L 01010001 00110101
928.
    +
    ALPHA:
    . ( 030) ALPHA          SAVE BETA REGS AND LOAD ALPHA SET
    . 27.50 (1.35 IF ALPHA)
    .
    .
    .
    . (111 030) ALPHAL      LOAD REGS FROM ALPHA SAVE AREA
    . 13.15                 FXLHEDCBA <- 'FXLHEDCBA'
    .
    . (062 030) SYSRET      RESTORE REGS AND RETURN
    . 21.00 (+ 0.40 IF BETA) PC <- (SP+1 | SP); SP <- SP + 2
    .                       FXLHEDCBA <- "FXLHEDCBA"
    .
    . NOTE: CAN NOT IMS. INTERRUPT BETWEEN ALPHA & FOLLOWING INSTRUCTION.
    .
    . TSTIP ,SWUSER,PSWI    ONLY IF PRIVED
    .
    . BRA IVIOL$,FZ
    . TSTIT ,SWRPT
    . BRA ALPHAL,FZ        IF REPEATED JUST DO SECOND HALF
    . BRA ALPHAL,T@,IO     NO SAVE, JUST DO ALPHA LOAD
    . BRA SYSRET,F@,IZ     RELOAD REGS & RETURN
    . TSTIT ,SWALBT        IS A SIMPLE ALPHA INSTRUCTION
    . BRA FTCHIAB,TZ       FORGET IT, ALREADY IN ALPHA MODE
    . DOPI ,PSWO,OR,SWRPT  MARK REPEATED BECAUSE 2 PARTS!
    .
    . BETAS LDTI SESAVBF.AND.0177 (7 BITS) TO POINT TO THE SAVE AREA
    . BRA MODSAV
    
```

```

929.
930. 001433L
931.
932.
933. 001433L 01101111 11110010          LDRT    TEMP2          SAVE AWAY FOR THE MOMENT
934. 001434L 00110001 11101010          LDX     SP2MRH         MSB STACK POINTER IS SAVE AREA ALSO
935. 001435L 00110001 11011011          DOTIP   ,ND,0200,SPIL  GET 128 BYTE BOUNDARY BIT (1 MSBIT)
    001436L 01010101 10000000
936. 001437L 01110011 11110010          DOPR    MAROL,OR,TEMP2  COMBINE WITH THE FLAG ADDRESS
    001440L 00110111 11000000
937. 001441L 00110001 00110101          DOPIP   MDW,ND,0303,UCFLG  SAVE THE FLAGS, ONLY 4 BITS OF INTEREST
    001442L 01010101 11000011
    001443L 00110111 00101001
938. 001444L 01010001 00010000          REGSVLP LDPI     LIMP,IMP8          INIT COUNT
    001445L 00110111 00000001
939.
940. 001446L 11010100 11011001          MODSVLP MWAIT   ,MEMPF1
    001447L 11010111 00010001
941. 001450L 00110111 00001101          STB     DMAR,DIMP      SAVE THE REGISTER
    001451L 00110111 00001001
942. 001452L 00110001 11011111          LDPP    MDW,IMPI
    001453L 00110111 00101001
943. 001454L 11011000 11011001          BRA     MODSVLP,F@,IZ   LOOP TILL ALL 8 REGS. ARE SAVED
944.
945. 001455L 00110001 11011100          TSTIP   ,SWRPT,PSWI    WELL, ONE OR TWO PARTS?
    001456L 01000101 00100000
946. 001457L 11010011 10111010          BRA     FTCHABW,TZ     ONLY SYSSAV, NO-LOAD NEW REGS.
947. 001460L 01010101 11111110          DOPI    MODW,ND,-1-SWINT  TEMPORARILY DISABLE INTERRUPTS FOR IT
    001461L 00110111 00000100
948.
949. 001462L 00110001 00110000          TSTPT   FI,SRVREQ      ANY REQUESTS PENDING?
950. 001463L 11010010 10111100          BRA     MODSRV,FZ      YES, DO THEM AND I HOPE NO TROUBLE
951. 001464L 00110001 11011100          TSTIP   ,SWALBT,PSWI   WHAT WAS IT?
    001465L 01000101 10000000
952. 001466L 11010100 11001001          MWAIT   ,MEMPF1       NEEDED AFTER MDW AT END OF LOOP ABOVE
    001467L 11010111 00010001
953. 001470L 11010010 10011100          BRA     ALPHAL,FZ      WAS BETA, DO ALPHAL NOW
954.                                BRA     BETAL          WAS ALPHA DO BETAL NOW
    
```

NO DSN 64K

*STOP SW64K, SWD
 BRA MOD SW64K, T2
 LDPR STW, SSTKPR*

. REGL, ALPHA, BETA MODE SWAPS AND SUB-PARTS

TSTIP SW 64K, PSWI
BBA BETA LN 64K, TZ
LDPR STW, SSTKPE

955.
956. 001471L
957.
958.
959.
960. 001471L 00110001 11101010
961. 001472L 00110001 11011011
001473L 01010101 10000000
962. 001474L 01010011 00110101
001475L 00110111 11000000
963. 001476L 00110111 01000111
964. 001477L 00110001 11011100
001500L 01010011 10000000
965. 001501L 01010101 11011111
966. 001502L 11011111 10010100
967.
968. >001503L 01011001 11111111
>001504L 11001111 11111111
969.
970. >001505L 01011001 11111111
>001506L 11001111 11111111
971.
972. 001507L
973.
974.
975.
976.
977.
978.
979.
980.
981.
982.
983.
984.
985.
986.
987.
988.
989.
990.
991. 001507L 01010001 00001001
001510L 00110111 00000001
992. >001511L 01011001 11111111
>001512L 01010001 11111111
>001513L 11001111 11111111
993.
994. 001514L
995.
996. 001514L 00110001 11001001
001515L 00110001 11101000
001516L 00110111 00001101

+
BETAL
. (111 020) BETAL LOAD REGS FROM BETA SAVE AREA
. 12.70 (HERE ON) FXLHEDCBA ← "FXLHEDCBA"

LDX SP2MRH
DOTIP ,ND,0200,SPIL

DOPI MAROL,OR,SESAVBF.AND.0177 POINT TO BETA FLAGS IN SAVE AREA

BETALN64K STB SMR
DOTIP ,OR,SWALBT,PSWI SET BETA MODE

DOTI ,ND,-1-SWRPT RESET REPEAT FLAG (IF SET)
BRA MODL0D

MODSRV BRAX SRVDO GO TO SERVICE AS NEEDED (MODSAV USES IT)

FTCHABW BRAX FETCHW *S* DO FETCH WAIT AT THE END

*
SYSRET
.* NOTE: THIS INSTRUCTION IS VERY LONG IN EXECUTION
.* IF DMA SLOWS IT EVEN FARTHER WE MAY HAVE PROBLEMS

.* WARNING: IF AS SOLUTION TO LENGTH IT IS DONE AS REPEATED INSTRUCTON
.* THEN: IF INTERRUPTED (I.E. BY RESTART-DEBUG INTERRUPT)
.* THE PC WILL REFLECT THE ADDRESS OF THE INSTRUCTION TO RETURN
.* TO, WITH REPEATED FLAG ON AND THE INCORRECT REGISTER SET IN THE
.* SUPPORT REGISTERS (THE ALPHAL OR BETAL NOT COMPLETED!)
.* THIS IS VERY BAD! BUT POSSIBILITY IS LOW AND NO SOLUTION SEEN

.* WARNING: IF INSIDE SYSRET (REGISTER LOAD PART) THERE IS A MEMORY FAULT,
.* THE PC WILL BE INCORRECT BECAUSE OF A SPECIAL PRE-DECREMENT.
.* IF THE IMP WAS NON-ZERO, IT WILL BE EVEN FARTHER OFF

. (062 030) SYSRET SYSTEM RETURN (FROM SC, BP, ETC)
. 20.15 (+ 0.40 IF BETAL) HERE ON PC ← (SP+1 | SP); SP ← SP + 2
. FXLHEDCBA ← "FXLHEDCBA"

LDPI LIMP,PCL GET THE RETURN ADDRESS INTO THE P.C.

BRC *POPSTO*,,SYSRET *SYSPOP* OFF PAGE WITH SPECIAL RETURN

SYSRET1:
. 15.55 + IF BETAL, HERE ON
DLDX PC2MR,,DMAR ASSUME ENTERED INST LEGALLY, (PRIVD)
SO, COMPLETE IT LEGALLY IN PRIV'D MODE
CORRECT FOR IMAR IN FETCH CODE

997. 001517L 00110001 10001001
 001520L 00110001 10101000
 998. 001521L 00110001 11101010
 999. 001522L 01010001 11000000
 1000. 001523L 00110101 11001011
 1001. 001524L 00110111 00001101
 1002. 001525L 00110001 11011100
 001526L 01010101 11111011
 001527L 00110111 00000100
 1003. 001530L 00110111 01000111
 1004. 001531L 01010101 00011000
 001532L 01101111 11110001
 1005. 001533L 01010001 11100111
 1006. 001534L 11010100 10100011
 001535L 11010111 00010001
 1007. 001536L 00110101 00110110
 1008. 001537L 01110011 11110001
 001540L 00110111 10001100
 1009.
 1010. 001541L 01000101 10000000
 1011. 001542L 11010010 11000110
 1012.
 1013.
 1014. 001543L
 1015.
 1016.
 1017.
 1018. 001543L 00110001 11101010
 1019. 001544L 00110001 11011011
 001545L 01010101 10000000
 1020. 001546L 01010011 00111110
 001547L 00110111 11000000
 1021. 001550L 00110111 01000111
 1022. 001551L 00110001 11011100
 001552L 01010101 01011111
 1023.
 1024.
 1025. 001553L
 1026.
 1027.
 1028.
 1029. 001553L 00110111 10001100
 1030. 001554L 00010111 10110010
 1031. 001555L 11010100 10010010
 001556L 11010111 00010001
 1032. 001557L 00110111 00001101
 1033. 001560L 00110001 00110110
 001561L 00110010 00110110
 1034. 001562L 00110111 00000110
 1035. 001563L 11011111 01100100

DLDX MR2PC
 LDX SP2MRH
 LDTI 0300
 DOP SP2MRL,ND
 STB DMAR
 DOPIP MODW,ND,-1-SWUSER,PSWI
 STB SMR
 DORIP TEMP1,ND,SWIRIM+SWSTDT
 LDTI -1-SWIRIM-SWSTDT
 MWAIT ,MEMPF1
 DOTP ,ND,MDR
 DOPR PSWO,OR,TEMP1
 TSTIT ,SWALBT
 BRA BETAL,FZ
 BRA ALPHAL
 *
 ALPHAL
 * (111 030) ALPHAL
 * 12.40 (HERE ON)
 LDX SP2MRH
 DOTIP ,ND,0200,SPIL
 DOPI MAROL,OR,SESAVAF.AND.0177 ONLY 7 BITS OF INTEREST
 STB SMR
 DOTIP ,ND,-1-SWRPT-SWALBT,PSWI
 BRA MODL0D
 *
 MODL0D
 * 11.35
 * NOTE: IF MACRO LEVEL PLAYS WITH FLAG BYTE, IT BETTER DO IT CORRECTLY
 LDPT PSWO
 CCLR
 MWAIT ,MEMPF1
 STB DMAR
 DOTPP ,AC,MDR,MDR
 STB LUF
 BRA MODL0P

GET THE PSW TO BE LOADED FROM THE SYSTEM SAVE AREA REMEMBER OLD RIM MODE INFO
 GET ALL THE OTHER STATUS BITS GET NEW PSW & DO NOT SET IT OR BAD THINGS
 MAY HAPPEN IF STACK IN PROTECTED MEMORY WHICH WAY TO GO? WHICH WAY TO GO?
 TO BETA!
 TO ALPHA
 LOAD REGISTERS FROM ALPHA SAVE AREA
 FXLHEDCBA ← 'FXLHEDCBA'

SW64K
 SYSRET 64K, TZ
 STW, SSTKPE

TSTIT ,SW64K
 BRA SYSREGT, TZ
 LOP 17,16,15
 LOP PSWI

TSTIP ,SW64K, PSWI
 BRA ALPHAN64K, TZ
 LOP STW, SSTKPE
 LOP PSWI

5X1RET64K

0200

```

1038.
1039. 001564L
1040.
1041.
1042.
1043.
1044.
1045.
1046. 001564L 11011000 01100110
1047. 001565L 00110001 11011100
      001566L 01010101 11111011
      001567L 00110111 00000100
1048. 001570L 00110001 11101010
      001571L 00110001 11001011
      001572L 00110111 01000111
1049. 001573L 11001110 11111111
      001574L 11010100 10000011
      001575L 11010111 00010001
1050. 001576L 00110001 00110110
      001577L 01101111 10110010
1051. 001600L 01010100 00001000
      001601L 00110111 00101001
1052. 001602L 11001110 11111111
      001603L 11010100 01111100
      001604L 11010111 00010001
1053. 001605L 00110111 00001100
1054. 001606L 11011111 01111000
1055. 001607L 00110111 01000111
1056. 001610L 11001110 11111111
      001611L 11010100 01110110
      001612L 11010111 00010001
1057. 001613L 00110001 00110110
      001614L 01101111 11110001
1058. 001615L 01010100 00000000
      001616L 00110111 00101001
1059. 001617L 01110001 11110010
1060. 001620L 11010100 01101111
      001621L 11010111 00010001
1061. 001622L 00110111 11000000
1062. 001623L 01110001 11110001
      001624L 00110111 11100000
      001625L 00110111 00001100
1063. 001626L 00110001 11011100
      001627L 00110111 00000100
1064. 001630L 11011111 11011011

```

```

*
REGS:
. 18.00 ( 055) REGS REGISTER SAVE
. (SP-7 | SP) <- XLHEDCBA; SP <- SP - 8
.
. 10.45 (111 055) REGL REGISTER LOAD
. XLHEDCBA <- (HL-7 | HL)
.
BRA REGL,F@,IZ DO REGISTER LOAD NOT SAVE!
DOPIP MODW,ND,-1-SWUSER,PSWI ALLOW STACK ACCESS TO PROTECTED MEM.
.
DLRX SP2MR,.,SMR GET TOP ENTRY ON THE STACK
.
MWAIT NOOP, MEMPF1
.
LDRP TEMPL,MDR,CC SAVE LSB OF POINTER
.
DOPI MDW,SB,8 UPDATE TOS (ASSUMING REGS WORKS)
.
MWAIT NOOP, MEMPF1
.
STB IMAR GET MSB OF TOS
DELAY 2
STB SMR
MWAIT NOOP, MEMPF1
.
LDRP TEMPH,MDR SAVE MSB OF POINTER
.
DOPI MDW,SB,0 UPDATE TOS (ASSUMING REGS WORKS)
.
LDTR TEMPL GET ORIGINAL (SAVED) LSB
MWAIT ,MEMPF1
.
LDPT MAROL LOAD THE MAR WITH THE INITIAL TOS
LDPR MAROH,TEMPH,IMAR AND CORRECT FOR THE FIRST DMAR
.
LDPP MODW,PSWI RESTORE THE CORRECT MODE
.
BRA REGSVLP AND GO SAVE ALL THE REGS

```

TSTIT ,SW64K
BAAA REGSNEND,TZ
LDPR STW, SSTRPE
STB SMR

TSTIT ,SW64K
BAAA REGSNEND,TZ
LDPR STW, USTRPE

```

1065.
1066. 001631L
1067.
1068.
1069.
1070. 001631L 00110001 11100101
      001632L 00110001 11000110
1071. 001633L 01010001 00010000
      001634L 00110111 00000001
1072. 001635L 00110111 01000111
1073. 001636L 00110001 00110110
      001637L 00110111 10001111
      001640L 00110111 00001001
1074. 001641L 11010100 01011110
      001642L 11010111 00010001
1075. 001643L 00110111 00001101
1076. 001644L 11011000 01100010
1077. 001645L 00110001 00110110
      001646L 00110111 10001111
1078. >001647L 01011001 11111111
      >001650L 11001111 11111111

```

```

+
REGL
• 10.45 (111 055) REGL REGISTER LOAD
•          BNA SYSSTL, FR, IO XLHEDCBA <- (HL-7 | HL)
          DLRX HL2MR INIT HL TO MAR
MODLOP LDPI LIMP,IMP8 INIT COUNTER (FIRST IMPO TO A-REG!)
REGLLP STB SMR
          LDPP IMPO,MDR,DIMP GET DATA & COUNT DOWN (WILL BE WASTED)
          MWAIT ,MEMPT
          STB DMAR
          BRA REGLLP,Fe,IZ LOOP FOR THE FULL COUNT
          LDPP IMPO,MDR FINALLY GET THE REAL A-REG VALUE
          BRAX FETCHRW RESTORE CORRECT MODE (FOR SYSRET)
          WS

```

10.45

SYS PSH where best
SYS POP where best

. SECTOR TABLE LOAD

```

1081.
1082. 001651L
1083.
1084.
1085.
1086.
1087.
1088.
1089.
1090.
1091.
1092.
1093.
1094.
1095.
1096.
1097. 001651L 00110001 11011100
      001652L 01000101 00000100
1098. 001653L 11000010 00100100
1099. 001654L 01010101 00100000
1100. 001655L 11010011 01001000
1101.
1102. 001656L 00110001 11010010
      001657L 01010101 00000111
      001660L 01101111 11110010
1103.
1104. 001661L 00010111 10100010
1104. 001662L 00010111 10100010
1104. 001663L 00010111 10100010
1104. 001664L 00010111 10100010
1105. 001665L 01010011 00001000
1106. 001666L 11011111 01000100
1107.
1108. 001667L 01101111 11110010
1109. 001670L 00110001 11010010
      001671L 01010101 00001111
1110. 001672L 11000011 10010100
1111.
1112. 001673L 11011001 00111111
1113. 001674L 01101111 11110001
1114. 001675L 00110001 11011111
      001676L 01010101 11110000
1115. 001677L 01110010 00110001
1116.
1117. 001700L 01101111 11110001
1118. 001701L 00110001 11010110
      001702L 01110010 00110010
      001703L 00110111 11000000
1119. 001704L 00110001 11010101
      001705L 01101111 11110010
1120. 001706L 00110110 11100000
1121. 001707L 00110111 10000101

```

*
STL:
. (077) STL LOAD THE SECTOR TABLE
. 5.40 + C * 2.50 (+0.55 IF C>8, OR 1.50 IF C=0)
. STL (0..C) <- (HL+C | HL); STL (15) <- SYS
. (022 077) STLOA LOAD WITH OFFSET
. (111 077) STLOB STL (R..R+C) <- (HL+C | HL)
. (062 077) STLOC STL(15) <- SYSROM
. (113 077) STLOD
. (174 077) STLOE
. 5.70 + C * 2.5 (+0.55 IF C>8, OR 1.50 IF C=0)
. NOTE: DOES NOT CHANGE HL OR C-REGISTERS
. NOTE: IN STLO'C', LOW 4 BITS COUNTER & HIGH 4 BITS OFFSET!
TSTIP ,SWUSER,PSWI ONLY IF PRIVED
BRA IVIOL\$,FZ
TSTIT ND,SWRPT,,TW ASSUME WILL BE ZERO, NOT REPEATED
BRA STLNRPT,TZ WAS NOT REPEATED
DORIP TEMP2,ND,07,URI+URC REPEATED, GET THE HL (MAR) BIAS AND
RPT 4
SHIFT SL THE POINTER BIAS AND COUNT FOR THE
SHIFT SL THE POINTER BIAS AND COUNT FOR THE
SHIFT SL THE POINTER BIAS AND COUNT FOR THE
SHIFT SL THE POINTER BIAS AND COUNT FOR THE
DOTI ,OR,010 FINAL EIGHT STL LOADS
BRA STLRPTD
STLNRPT LDRT TEMP2 REGULAR HL (MAR) NEEDS NO BIAS
TSTIP ,017,URI+URC,TW GET THE COUNT OF THE STEPS TO DO
BRA FTCHIAB,TZ IF ZERO, WAS NOTHING TO DO. SO, THE END
STLRPTD BRA STLZRO,T@,IZ DO STANDARD STL
LDRT TEMP1 SAVE AWAY
DOTIP ,ND,0360,IMPI IMP STL STARTS STL WITH OFFSET
DOTR ,AC,TEMP1,,CO COMBINE GIVEN OFFSET WITH BIAS
STLZRO LDRT TEMP1 SAVE THE POINTER/COUNTER AS GENERATED
DOPRP MAROL,AC,TEMP2,URI+URL,CO BIAS TABLE ADDRESS (IF NEEDED)
LDRP TEMP2,URI+URH SAVE AWAY URH SO CAN BE RESTORED
DOP MAROH,IT
LDPT URO+URH IN CASE TABLE CROSSES PAGE BOUNDARY

1122.	001710L 00110111 01000111	STB	SMR	GET NEXT (FIRST) TABLE ENTRY	
1123.					
1124.	001711L 01110001 11110001	STLAGN	LDTR	TEMP1	GET THE INITIAL VIRTUAL ADDRESS
1125.					
1126.	001712L 11010100 00110101	STLOOP	MWAIT	,STLDONE	RESTORE REGS & SET VECTOR FIRST
	001713L 11010111 00011110				
1127.	001714L 00110111 11100000		LDPT	MAROH	LOAD VIRTUAL ADDRESS FROM TEMP
1128.	001715L 01010001 00000010		LDPI	MODW,SWBASD	DISABLE BASING (AND 1 MS INTERRUPTS)
	001716L 00110111 00000100				
1129.	001717L 00110001 00110110		DOPIP	STW,ND,0375,MDR	SET PHYSICAL SECTOR # IN VIRTUAL LOCN.
	001720L 01010101 11111101				
	001721L 00110111 00000101				
1130.	001722L 00110001 11100101		LDX	HL2MRH,IMAR	RESTORE MARH FROM H SAVE AREA
	001723L 00110111 00001100				
1131.	001724L 00110001 11011100		LDPP	MODW,PSWI	RESTORE BASING (1 MS INT. 1 INST. DELAY
	001725L 00110111 00000100				
1132.	001726L 00110111 01000111		STB	SMR	GET NEXT TABLE ENTRY
1133.	001727L 00110001 10100101		LDX	MR2HLH	SAVE MARH IN H
1134.	001730L 01110001 10110001		DORIR	TEMP1,AC,017,TEMP1,CC	INC VIRTUAL SECTOR # & DECR COUNT
	001731L 01010010 00001111				
	001732L 01101111 11110001				
1135.	001733L 01000101 00000111		TSTIT	,07	AT SPLIT POINT?
1136.	001734L 11010010 00110101		BRA	STLOOP,FZ	NO, CONTINUE
1137.					LOOPING JUMP IS DURING MEMORY READ
1138.					THIS MAKES EXEC FASTER.
1139.	001735L 01000101 00001111		TSTIT	,017	REALLY FINISHED?
1140.	001736L 11010011 00011110		BRA	STLDONE,TZ	YES, CLEANUP AND END
1141.	001737L 00110001 00110000		TSTPT	FI,SRVREQ	NO, ANY SERVICE TO DO?
1142.	001740L 11010011 00110110		BRA	STLAGN,TZ	NO, THEN DO SECOND HALF NOW
1143.					REPEATED! WILL DO SERVICE BEFORE SECOND
1144.					PART BUT DO CLEANUP FIRST
1145.	001741L 11010100 00011110	STLDONE	MWAIT	,S+1	RESTORE BEFORE MEMPF
	001742L 11010111 00011100				
1146.					BUT NOTE: MAR MSB WILL BECOME INCORRECT
1147.	001743L 01110001 11110010		LDPR	URO+URH,TEMP2	RESTORE H-REG
	001744L 00110111 10000101				
1148.	001745L 01010001 11110000		LDPI	MAROH,SYSPROM>8.AND.0360	!! FORCE LAST ENTRY TO
	001746L 00110111 11100000				
1149.	001747L 00110111 00000101		LDPT	STW	ACCESS PROTECT AND WRITE PROTECT
1150.	>001750L 01011001 11111111		BPGX	RIND	
1151.	001751L 01110001 11110001		TSTIR	,017,TEMP1	REALLY FINISHED?
	001752L 01000101 00001111				
1152.	>001753L 11000011 11111111		BRA	RIND,TZ	YES, RESET REPEAT FLAG
1153.	>001754L 01011001 11111111		BRAX	SRVRPT	NO, DO IT AS REPEATED INST.
	>001755L 11001111 11111111				
1154.					(BOTH RIND & SRVRPT INDIRECT TO MEMPF)
1155.					. NOTE: THIS INSTRUCTION DOES AN EXTRA WASTED READ. BUT WHAT IF IT IS TO
1156.					ACCESS PROTECTED MEMORY (ACROSS SECTOR BOUNDARY)?
1157.					. NO PROBLEM, INSTRUCTION IS PRIV'D SO CAN'T GET THOSE VIOLATIONS
1158.					. BUT A REAL MEMPF OR STPE WILL CAUSE AN INTERRUPT.

. SECTOR TABLE LOAD

1159.
1160. >001756L 01011001 11111111
>001757L 11001111 11111111
1161.
1162. 001760L
1163. 001760L 00110001 10000110
001761L 00110001 10100101
1164. >001762L 010.11001 11111111
>001763L 11001111 11111111
1165.
1166. 001764L 11111111 1111.1111
001765L 11111111 11111111
001766L 11111111 11111111
001767L 11111111 11111111
001770L 1111.1111 1111.1111
001771L 11111111 11111111
001772L 11111111 1.111.1111
001773L 11111111 11111111
001774L 1111.1111 11111111
001775L 11111111 11111111
001776L 11111111 1111.1111
001777L 11111111 1111.1111
1167. 002000
1168. 000000
1169. 000000
1170. 000000

*
MEMPF1 BRAX MEMPFS

.
MIOEND FIT REMAINDER WHERE THERE IS ROOM
RESTORE REG PAIR

DLDX MR2HL

BRAX FETCH

TABPAGE PROCL

PROCLN EQU \$-PROCP
USE PROCL
SKIP PROCLN
END POR

	AC	121	155	163	218	219	312	436	517	672	1033	1115	1118
		1134											
010015	ACD	*35:I	108	164	166								
001051	ADRON	*598	594										
001417	ALPHA	*903											
001543	ALPHAL	*1014	921	922	953								
001413	ALPHAS	*893	900										
	B0	64:I											
	B1	65:I											
	B2	66:I											
	B3	67:I											
	B4	68:I											
	B5	69:I											
	B6	70:I											
	B7	71:I											
	BASW	107											
001400	BETA	*870											
001471	BETAL	*956	887	888	1011								
001432	BETAS	*927	901										
000744	BLKEND	*527	519	522									
000732	BLKGO	*521	518										
000751	BLKIN	*530											
000715	BLKLOOP	*511	546										
000675	BLKOUT	*495											
000742	BLKRPT	*526	524										
001312	BP	*780											
020006	BR	*19:I	449	461	473	476	487	491	506	539	542		
	C0	218	312	517	750	751	1115	1118					
	C1	130	166	294									
000000	CAP55IO	*70:I	73:I										
000060	CAPABILI	*73:I	385										
000000	CAPAPF	*67:I	73:I										
000000	CAPBLUE	*66:I	73:I										
000000	CAPCOM	*71:I	73:I										
000020	CAPDMPIO	*68:I	73:I										
000000	CAPIMA	*65:I	73:I										
000000	CAPMICR	*64:I	73:I										
000040	CAPRIM	*69:I	73:I										
	CC	112	164	215	402	437	520	670	715	726	759	1030	1050
		1104	1134										
007000	CDOR	*81:I											
006000	CDOX	*80:I											
	CF	108	109	127	130	150	156	176	179	181	184	219	257
		260	271	277	285	291	294	296	300	311	313	324	510
		544	672	688	749	776	799	800	805	807	835	836	933
		936	1004	1008	1057	1059	1062	1102	1108	1113	1117	1119	1124
		1134	1147	1151									
	CMPF	103											
001067	COM4X	*618	644										
	DE2MRH	515											
	DE2MRL	515											
	DIMP	356	374	380	420	941	1073						

